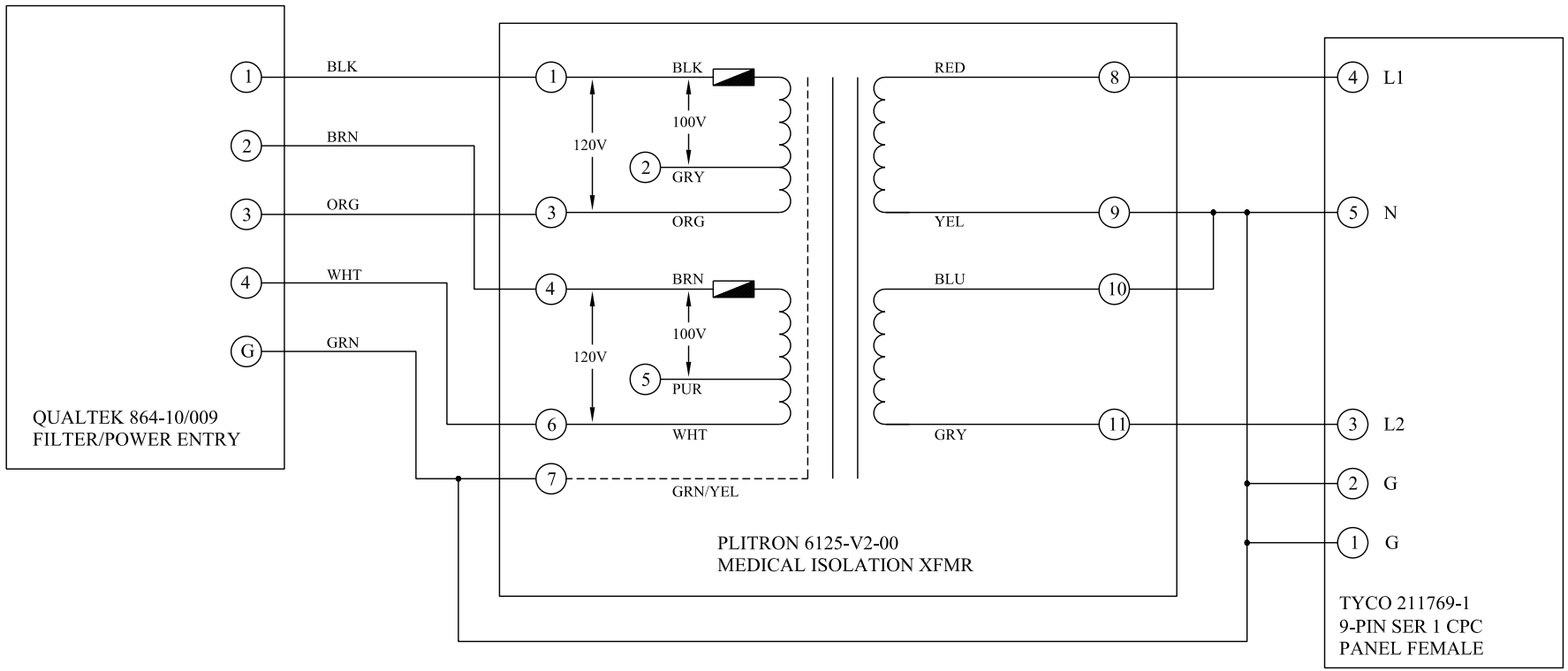

THE OHIO STATE UNIVERSITY

DEPT OF ASTRONOMY

NAME

KMT COMPUTER RACK
HE POWER DRAWER

MATERIAL	FINISH	GENERAL TOLERANCES DECIMALS .XX +/- .010 .XXX +/- .003	ANGULAR +/- 0 30'

DESIGNED BY DP	DATE 24MAR2014	DWG NO. ISOLATION XFMR WIRING	REV A
DRAWN BY DP	DATE 24MAR2014		
APPROVED BY XXX	DATE XX/XX/XX	SCALE:	

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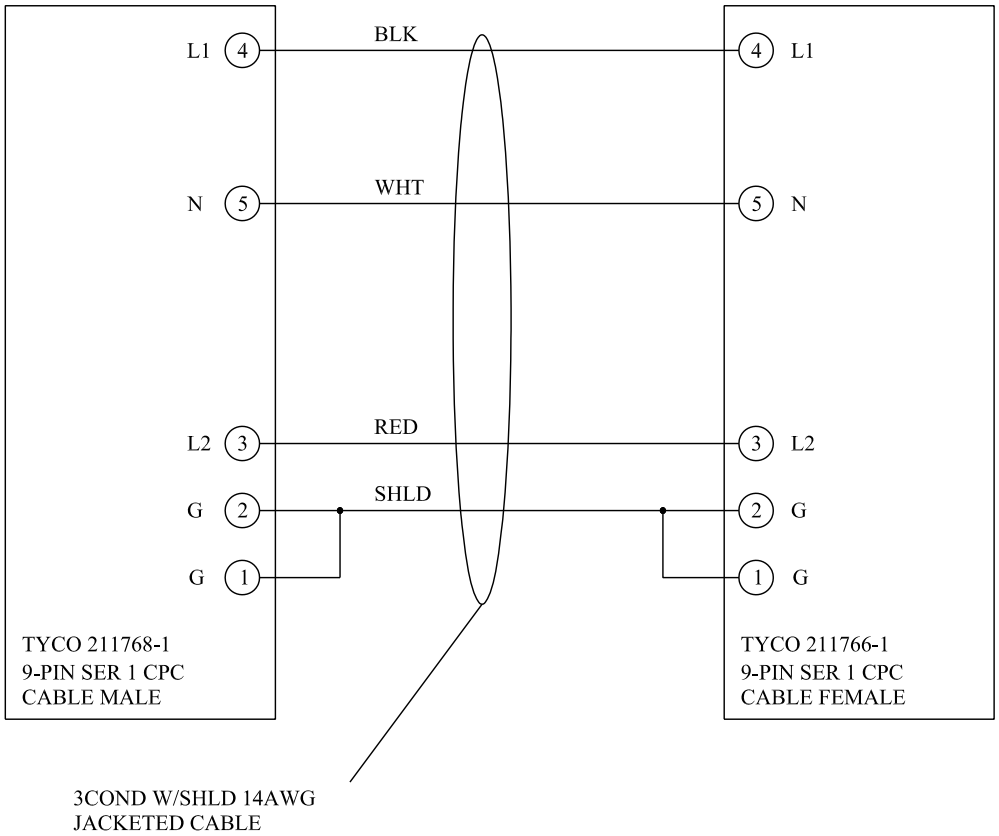
atwood



LENGTH = 150 FT

THE OHIO STATE UNIVERSITY

DEPT OF ASTRONOMY

NAME
KMT HE POWER CORD

MATERIAL	FINISH	GENERAL TOLERANCES DECIMALS .XX +/- .010 .XXX +/- .003 ANGULAR +/- 0 30'

DESIGNED BY DP	DATE 24MAR2014	DWG NO. HE Power Cable	REV A
DRAWN BY DP	DATE 24MAR2014		
APPROVED BY XXX	DATE XX/XX/XX	SCALE:	

C:\DOCUME~1\bceru\LOCALS~1\Temp\HE Power Cable_ACADR14.dwg, 6/18/2015 4:29:57 PM, 1:6.44336,
atwood

REVISION RECORD		

$$$49

MH1
6-32MHOLE

MH5
6-32MHOLE

MH6
6-32MHOLE

TP1
GND

MH4
6-32MHOLE

V1
V230LA20A

V2
V230LA20A

V3
V230LA20A

V4
V230LA20A

CON_PHOENIX_5
J1

CON_PHOENIX_4
J2

CON_PHOENIX_4
J3

CON_PHOENIX_4
J4

CON_PHOENIX_4
J5

CON_PHOENIX_4
J6

CON_PHOENIX_3
J8

V5
V230LA20A

V6
V230LA20A

V7
V230LA20A

V8
V230LA20A

CON_PHOENIX_4
J7

CON_PHOENIX_4
J9

CON_PHOENIX_4
J10

CON_PHOENIX_4
J11

CON_PHOENIX_4
J12

CON_PHOENIX_3
J13

MH3
6-32MHOLE

MH2
6-32MHOLE

COMPANY: THE OHIO STATE UNIVERSITY DEPARTMENT OF ASTRONOMY IMAGING SCIENCES LABORATORY					
TITLE: MODS Power Supply Board					
DRAWN: MOJ	DATED: 11.17.08	CODE:	SIZE: C	DRAWING NO: PowerSupplyBoard1	REV: A
CHECKED:	DATED:	SCALE: NONE		SHEET: 1 OF 2	

6 5 4 3 2 1

D C B A

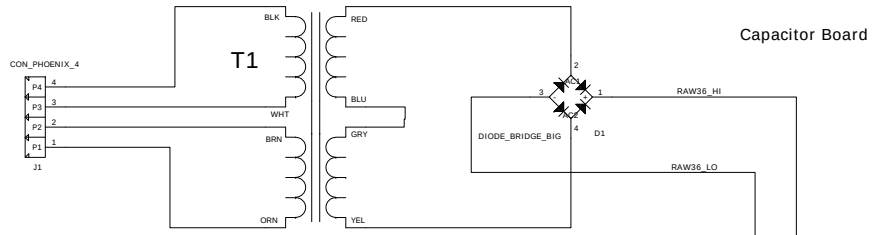
REVISION RECORD		

		COMPANY: THE OHIO STATE UNIVERSITY DEPARTMENT OF ASTRONOMY IMAGING SCIENCES LABORATORY			
		TITLE: MODS Power Supply Board			
DRAWN: MOJ	DATED: 11.17.08	CODE:	SIZE: C	DRAWING NO: PowerSupplyBoard1	REV: A
CHECKED:	DATED:	SCALE: NONE		SHEET: 2 OF 2	

REVISION RECORD		

1182J15 36V for CBBs

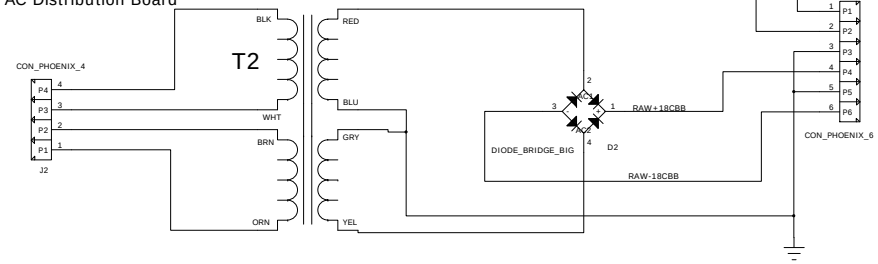
AC Distribution Board



Capacitor Board

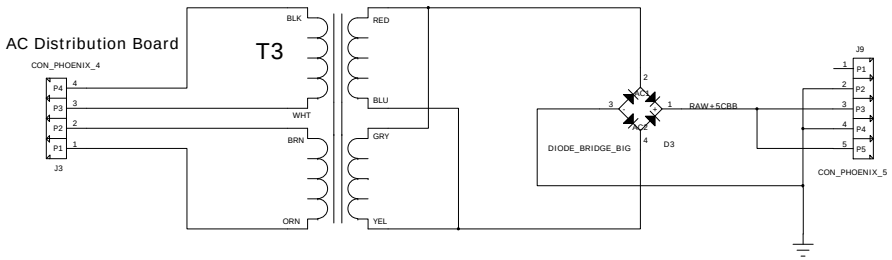
182N18 +/- 18 for CBB's

AC Distribution Board



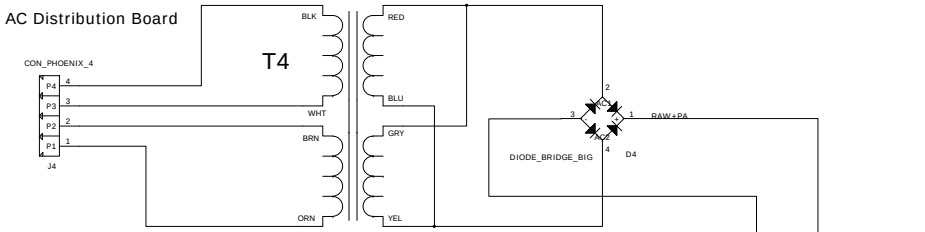
182N9 +5 for CBBs

AC Distribution Board



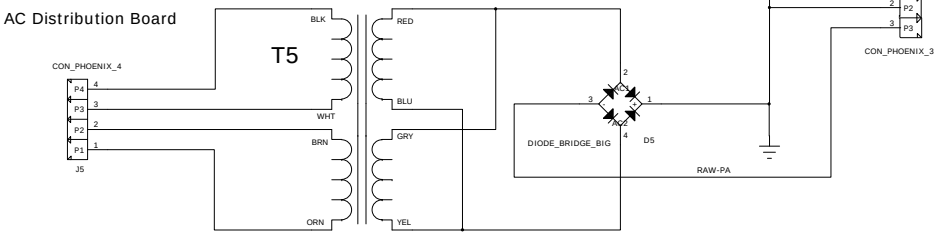
182N9 +PAV (7.5V)

AC Distribution Board



182N9 -PAV (7.5V)

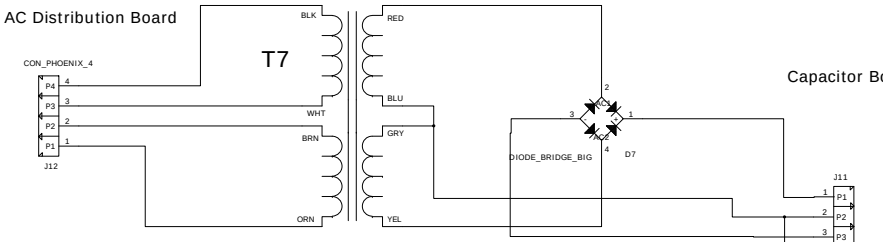
AC Distribution Board



Power Supply Board

182M15 +/- 15 Utility

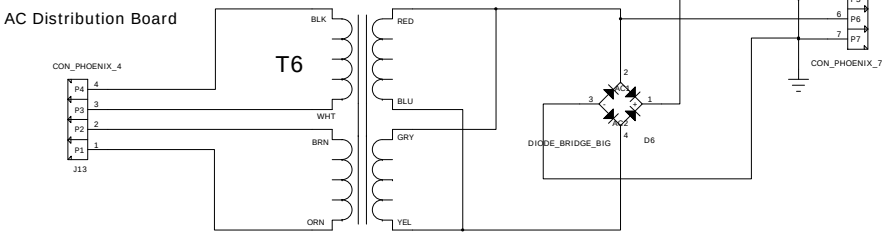
AC Distribution Board



Capacitor Board

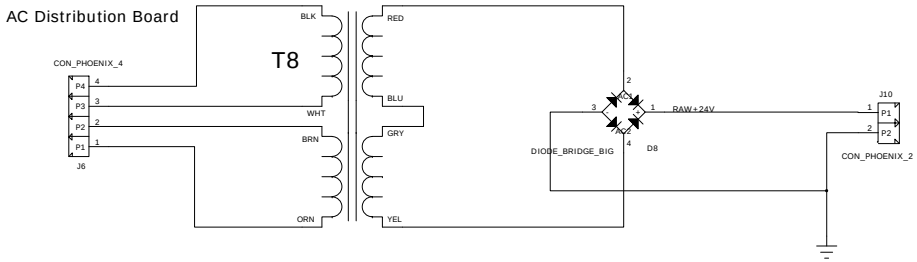
182M9 +5V Utility

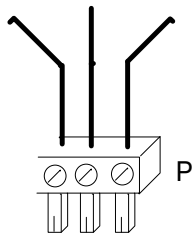
AC Distribution Board



1182Q12 +24 V for Utility Bd

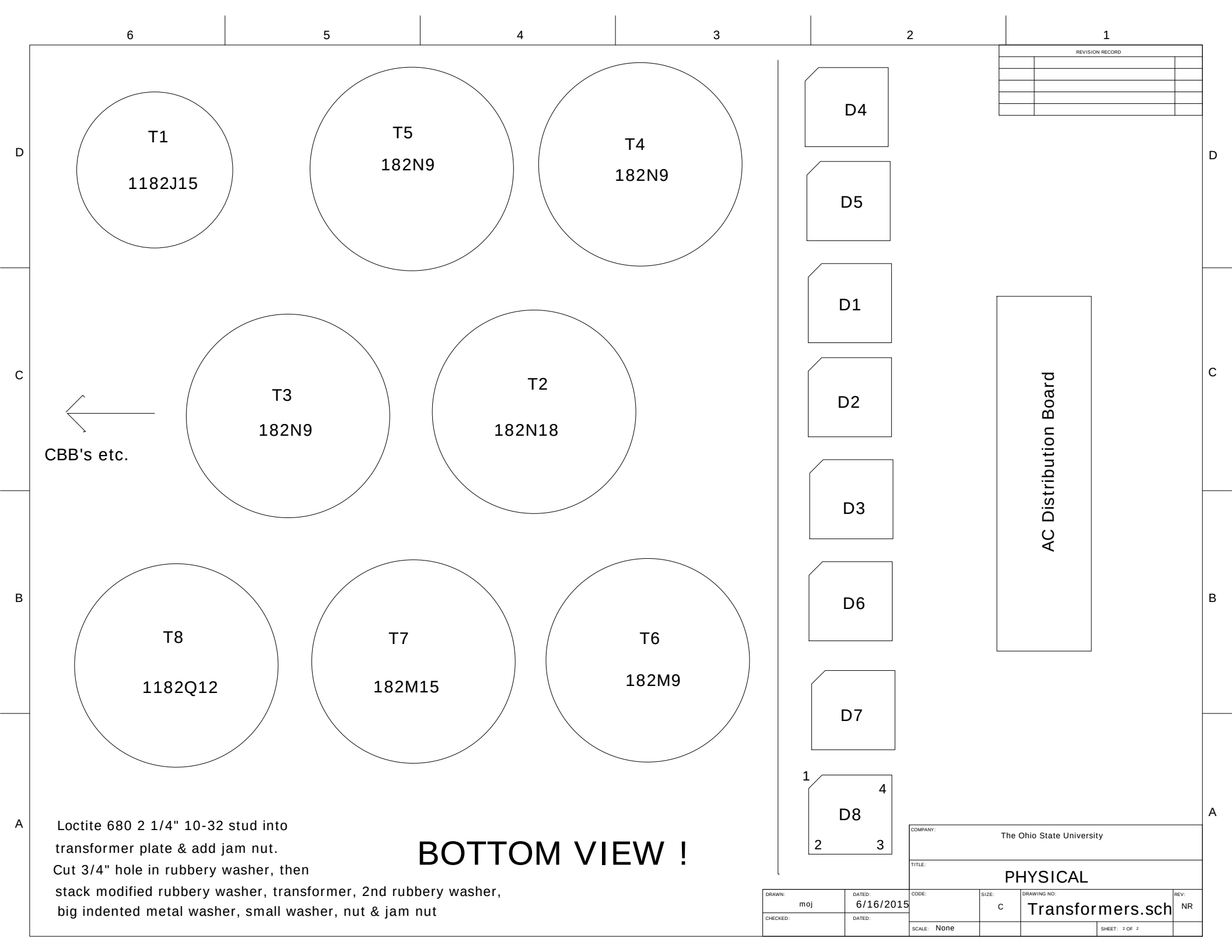
AC Distribution Board

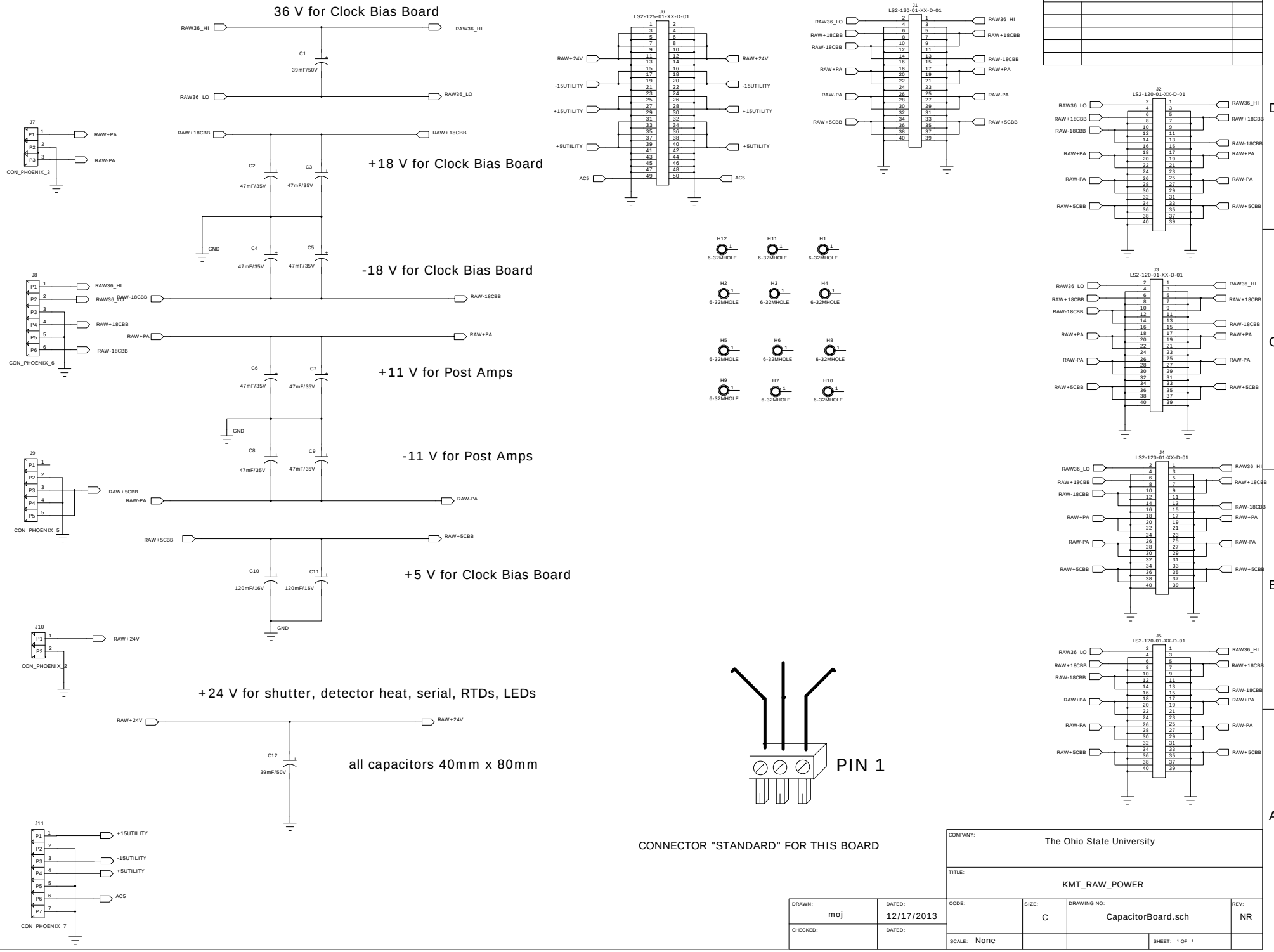


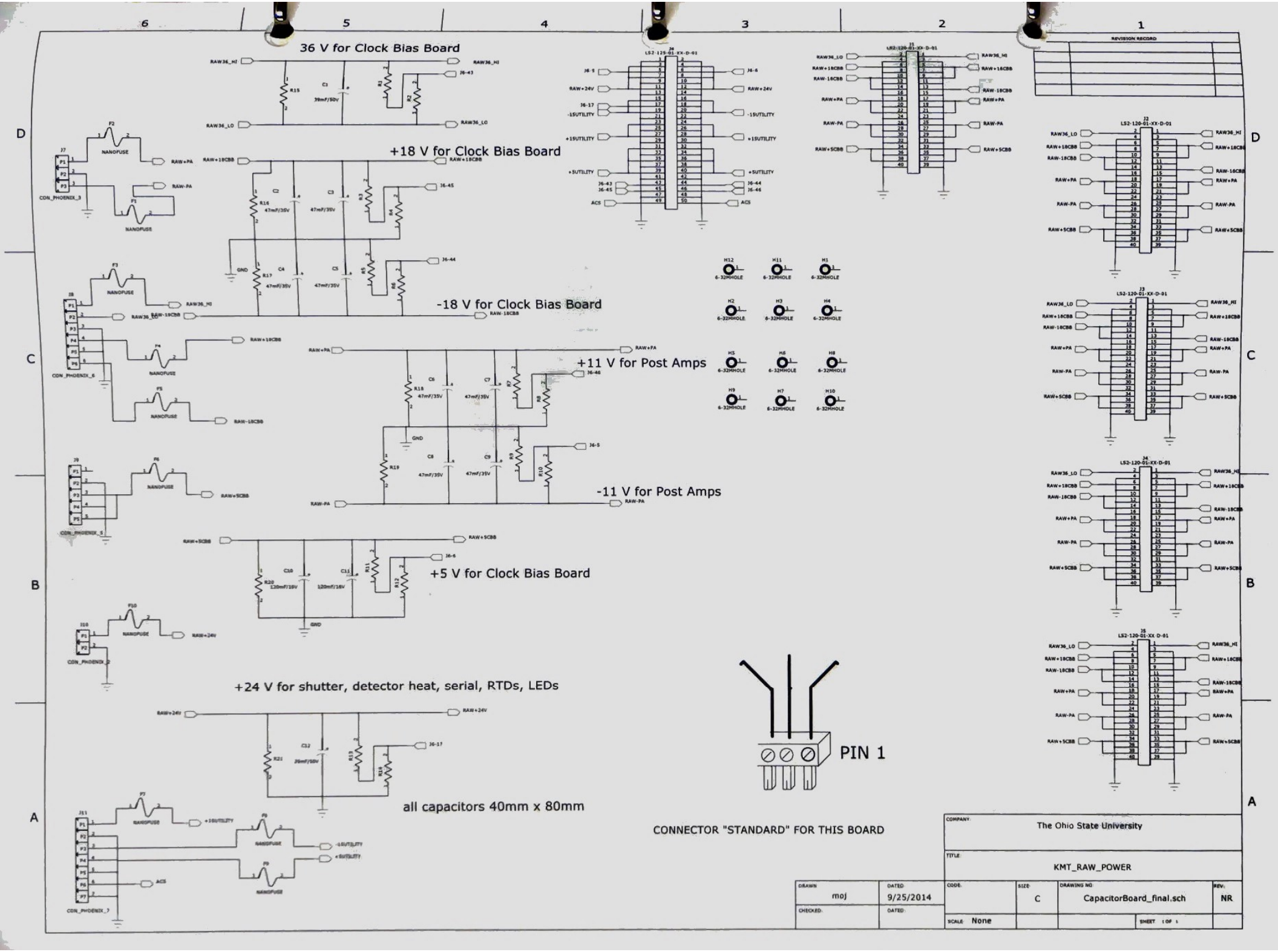


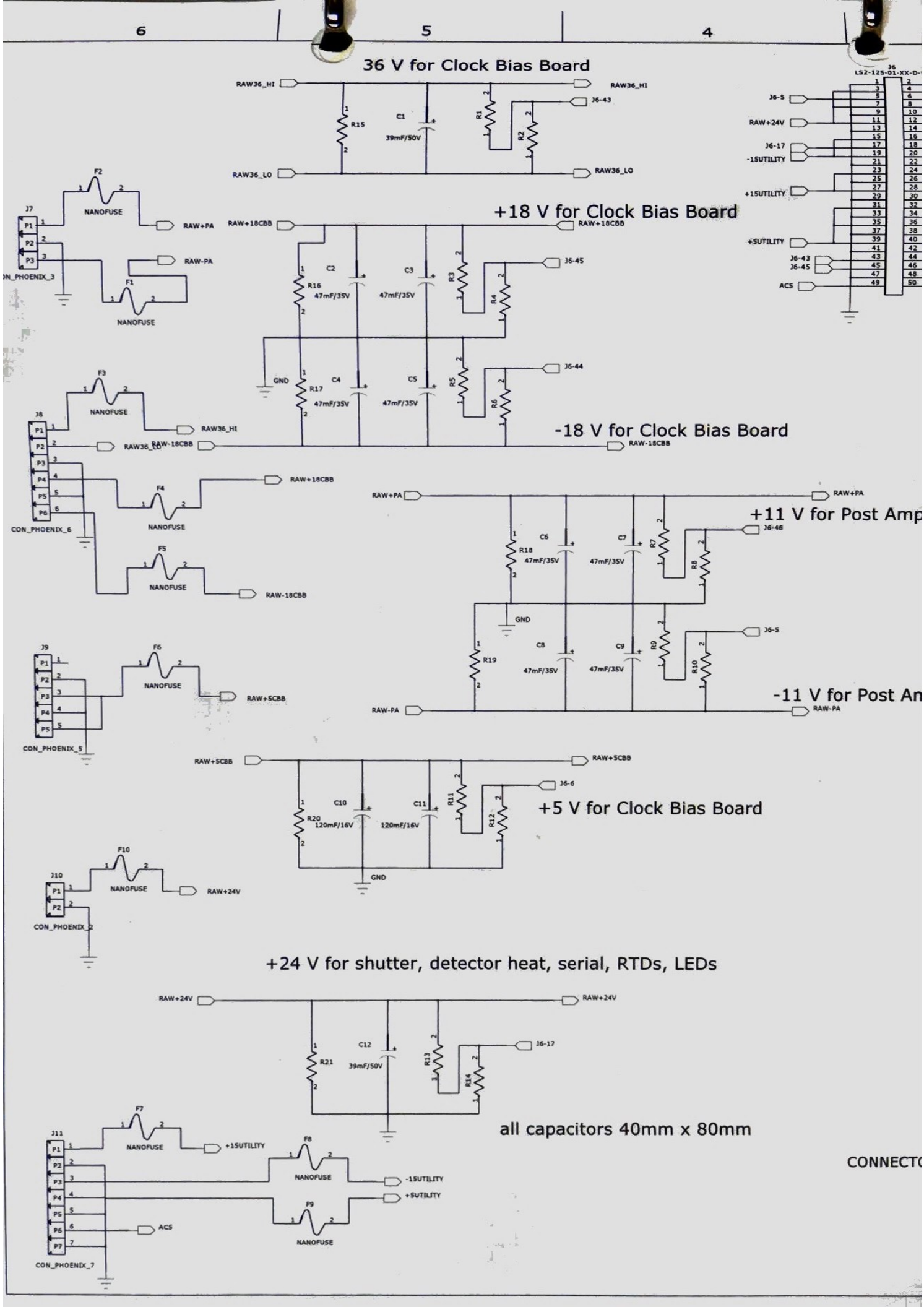
CONNECTOR "STANDARD" FOR THIS BOARD

COMPANY: The Ohio State University					
TITLE: ELECTRICAL					
DRAWN: moj	DATED: 6/16/2015	CODE:	SIZE: C	DRAWING NO: Transformers.sch	REV: NR
CHECKED:	DATED:	SCALE: None		SHEET: 1 OF 2	


6
5
4
3
2
1
REVISION RECORD
T1
1182J15
T5
182N9
T4
182N9
D4
D5
D1
D2
D3
D6
D7
D8
1
4
2
3
AC Distribution Board
T3
182N9
T2
182N18
CBB's etc.
T8
1182Q12
T7
182M15
T6
182M9
Loctite 680 2 1/4" 10-32 stud into
transformer plate & add jam nut.
Cut 3/4" hole in rubbery washer, then
stack modified rubbery washer, transformer, 2nd rubbery washer,
big indented metal washer, small washer, nut & jam nut
BOTTOM VIEW !
COMPANY: The Ohio State University
TITLE: PHYSICAL
DRAWN: moj
DATED: 6/16/2015
CHECKED:
DATED:
CODE:
SIZE: C
DRAWING NO: Transformers.sch
REV: NR
SCALE: None
SHEET: 2 OF 2

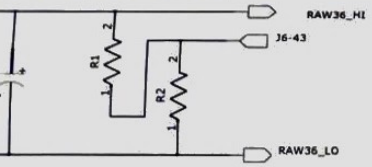

36 V for Clock Bias Board
+18 V for Clock Bias Board
-18 V for Clock Bias Board
+11 V for Post Amps
-11 V for Post Amps
+5 V for Clock Bias Board
+24 V for shutter, detector heat, serial, RTDs, LEDs
all capacitors 40mm x 80mm
PIN 1
CONNECTOR "STANDARD" FOR THIS BOARD
REVISION RECORD
COMPANY: The Ohio State University
TITLE: KMT_RAW_POWER
DRAWN: moj
DATED: 12/17/2013
CHECKED:
DATED:
CODE:
SIZE: C
DRAWING NO: CapacitorBoard.sch
REV: NR
SCALE: None
SHEET: 1 OF 1

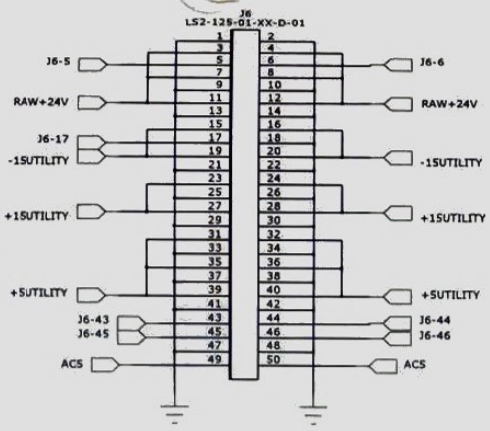

36 V for Clock Bias Board
+18 V for Clock Bias Board
-18 V for Clock Bias Board
+11 V for Post Amps
-11 V for Post Amps
+5 V for Clock Bias Board
+24 V for shutter, detector heat, serial, RTDs, LEDs
all capacitors 40mm x 80mm
PIN 1
CONNECTOR "STANDARD" FOR THIS BOARD
REVISION RECORD
COMPANY: The Ohio State University
TITLE: KMT_RAW_POWER
DRAWN: moj
DATED: 9/25/2014
CHECKED:
DATED:
CODE:
SIZE: C
DRAWING NO: CapacitorBoard_final.sch
REV: NR
SCALE: None
SHEET 1 OF 1

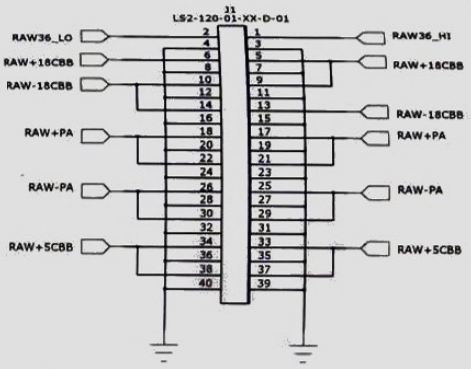

6
5
4
36 V for Clock Bias Board
RAW36_HI
RAW36_HI
J6-43
R15
C1
39mF/50V
R1
R2
RAW36_LO
RAW36_LO
J6
LS2-125-01-XX-D-
J6-5
RAW+24V
J6-17
-15UTILITY
+15UTILITY
+5UTILITY
J6-43
J6-45
ACS
F2
NANOFUSE
J7
P1
P2
P3
RAW+PA
RAW-PA
F1
NANOFUSE
+18 V for Clock Bias Board
RAW+18CBB
RAW+18CBB
J6-45
C2
C3
R16
47mF/35V
47mF/35V
R3
R4
GND
J6-44
C4
C5
R17
47mF/35V
47mF/35V
R5
R6
F3
NANOFUSE
J8
P1
P2
P3
P4
P5
P6
RAW36_HI
RAW36_LO
RAW-18CBB
RAW-18CBB
-18 V for Clock Bias Board
RAW+18CBB
F4
NANOFUSE
F5
NANOFUSE
RAW-18CBB
CON_PHOENIX_6
RAW+PA
RAW+PA
+11 V for Post Amp
J6-46
C6
C7
R18
47mF/35V
47mF/35V
R7
R8
GND
J6-5
C8
C9
R19
47mF/35V
47mF/35V
R9
R10
-11 V for Post An
RAW-PA
RAW-PA
J9
P1
P2
P3
P4
P5
F6
NANOFUSE
RAW+5CBB
CON_PHOENIX_5
RAW+5CBB
RAW+5CBB
J6-6
C10
C11
R20
120mF/16V
120mF/16V
R11
R12
+5 V for Clock Bias Board
GND
F10
NANOFUSE
J10
P1
P2
RAW+24V
CON_PHOENIX_2
+24 V for shutter, detector heat, serial, RTDs, LEDs
RAW+24V
RAW+24V
J6-17
C12
R21
39mF/50V
R13
R14
all capacitors 40mm x 80mm
F7
NANOFUSE
J11
P1
P2
P3
P4
P5
P6
P7
+15UTILITY
F8
NANOFUSE
-15UTILITY
+5UTILITY
F9
NANOFUSE
ACS
CON_PHOENIX_7
CONNECT

5 4 3 2

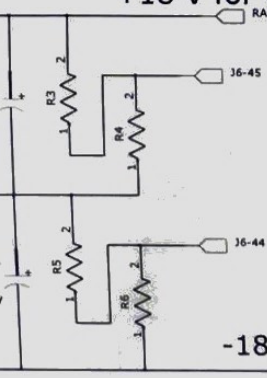
for Clock Bias Board

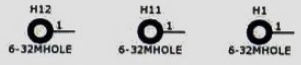


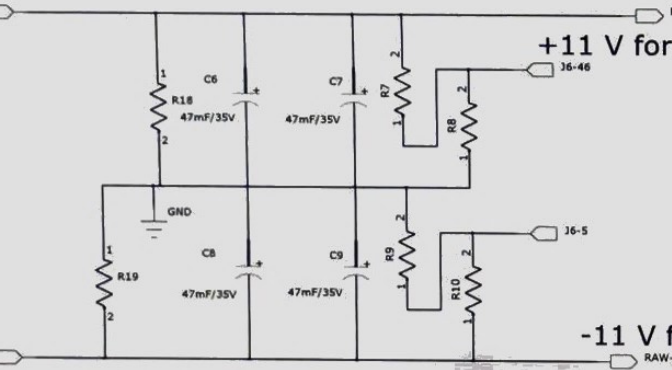




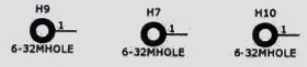
+18 V for Clock Bias Board

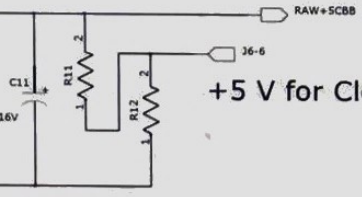


-18 V for Clock Bias Board

+11 V for Post Amps



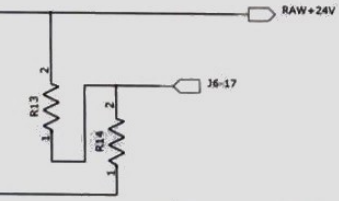
-11 V for Post Amps



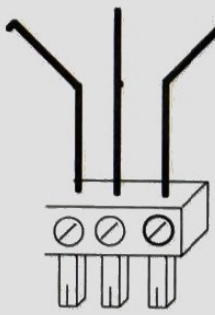


+5 V for Clock Bias Board

er, detector heat, serial, RTDs, LEDs



all capacitors 40mm x 80mm

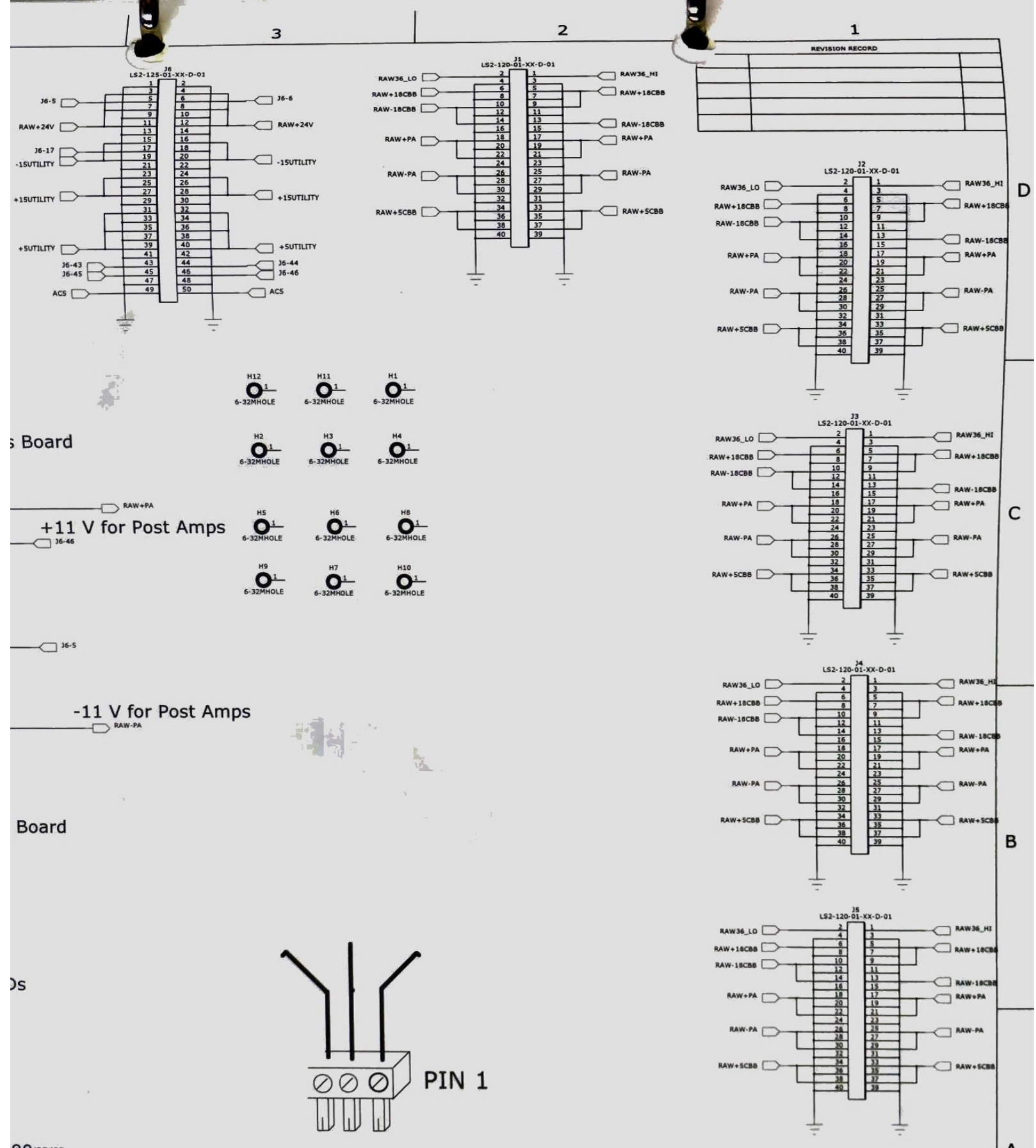


PIN 1

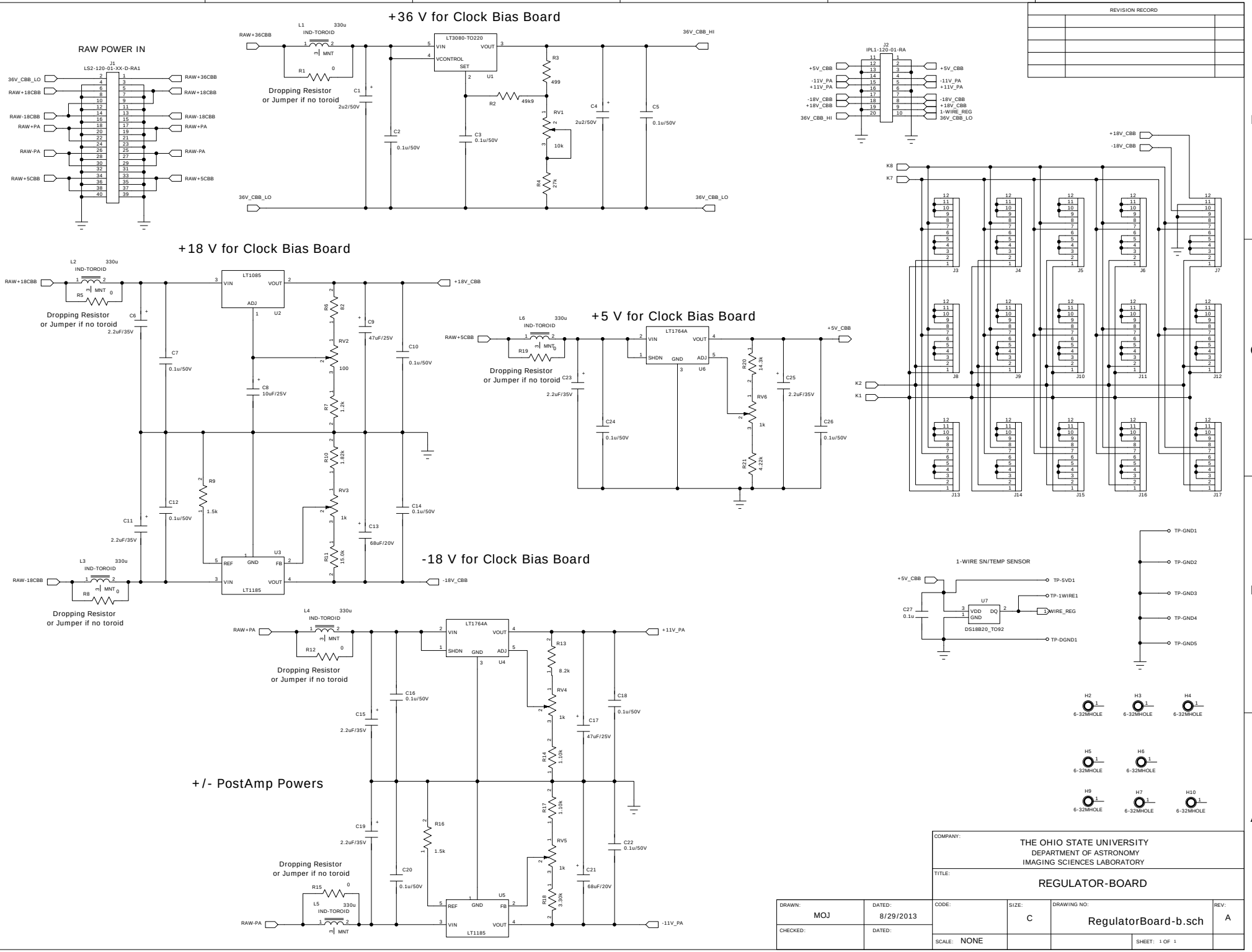
CONNECTOR "STANDARD" FOR THIS BOARD

-15UTILITY
+5UTILITY

COMPANY: The Oh			
TITLE: KM			
DRAWN: moj	DATED: 9/25/2014	CODE:	SIZE: C
CHECKED:	DATED:	SCALE: None	



COMPANY: The Ohio State University						
TITLE: KMT_RAW_POWER						
DRAWN: moj	DATED: 9/25/2014	CODE:	SIZE: C	DRAWING NO: CapacitorBoard_final.sch		REV: NR
CHECKED:	DATED:	SCALE: None			SHEET: 1 OF 1	


6
5
4
3
2
1
D
C
B
A
REVISION RECORD
+36 V for Clock Bias Board
RAW POWER IN
J1
LS2-120-01-XX-D-RA1
36V_CBB_LO
RAW+18CBB
RAW-18CBB
RAW+PA
RAW-PA
RAW+5CBB
RAW+36CBB
L1 330u
IND-TOROID
MNT
R1 0
Dropping Resistor
or Jumper if no toroid
LT3080-TO220
VIN
VOUT
VCONTROL
SET
U1
C1 2u2/50V
C2 0.1u/50V
C3 0.1u/50V
R2 49k9
R3 499
RV1 10k
R4 27k
C4 2u2/50V
C5 0.1u/50V
36V_CBB_HI
J2
IPL1-120-01-RA
+5V_CBB
-11V_PA
+11V_PA
-18V_CBB
+18V_CBB
1-WIRE_REG
+18 V for Clock Bias Board
L2 330u
IND-TOROID
R5 0
LT1085
ADJ
U2
+18V_CBB
C6 2.2uF/35V
C7 0.1u/50V
C8 10uF/25V
R6 82
RV2 100
R7 1.2k
C9 47uF/25V
C10 0.1u/50V
R10 1.82k
RV3 1k
R11 15.0k
R9 1.5k
C11 2.2uF/35V
C12 0.1u/50V
C13 68uF/20V
C14 0.1u/50V
U3
REF
GND
FB
LT1185
L3 330u
R8 0
-18V_CBB
-18 V for Clock Bias Board
+5 V for Clock Bias Board
L6 330u
R19 0
LT1764A
SHDN
U6
C23 2.2uF/35V
C24 0.1u/50V
R20 14.3k
RV6 1k
R21 4.22k
C25 2.2uF/35V
C26 0.1u/50V
K8
K7
K2
K1
J3
J4
J5
J6
J7
J8
J9
J10
J11
J12
J13
J14
J15
J16
J17
1-WIRE SN/TEMP SENSOR
U7
VDD
DQ
GND
DS18B20_TO92
C27 0.1u
TP-5VD1
TP-1WIRE1
TP-DGND1
TP-GND1
TP-GND2
TP-GND3
TP-GND4
TP-GND5
+/- PostAmp Powers
L4 330u
R12 0
U4
+11V_PA
C15 2.2uF/35V
C16 0.1u/50V
R13 8.2k
RV4 1k
R14 1.10k
C17 47uF/25V
C18 0.1u/50V
C19 2.2uF/35V
C20 0.1u/50V
R16 1.5k
R17 1.10k
RV5 1k
R18 3.30k
C21 68uF/20V
C22 0.1u/50V
R15 0
L5 330u
U5
-11V_PA
H2
H3
H4
H5
H6
H7
H9
H10
6-32MHOLE
COMPANY:
THE OHIO STATE UNIVERSITY
DEPARTMENT OF ASTRONOMY
IMAGING SCIENCES LABORATORY
TITLE:
REGULATOR-BOARD
DRAWN:
MOJ
DATED:
8/29/2013
CHECKED:
DATED:
CODE:
SIZE:
C
DRAWING NO:
RegulatorBoard-b.sch
REV:
A
SCALE: NONE
SHEET: 1 OF 1

Sang-Mok CHA

보낸 사람: "Bruce Atwood" <atwood.1@osu.edu>
날짜: 2015년 10월 15일 목요일 오후 1:58
받는 사람: "Daniel Pappalardo" <pappalardo.1@osu.edu>; "'Sang-Mok CHA'" <chasm@kasi.re.kr>
참조: "Jerry Mason" <mason.8@osu.edu>
제목: Re: Capacitor board resistors for read-back of raw voltages

On 6/19/2015 3:13 PM, Bruce Atwood wrote:

> Resistor values required on Cap Board to read back raw voltages. Gains are as used in ISATOTPS.bas
>
> | supply | series | to gnd | V for 2.5V | 1/Av | J6- | ADC | Pin# | |
> |---|---|---|---|---|---|---|---|---|
> | +36 | R1=42.2k | R2=2.21k | 50.24 | 20.10 | 43 | ADC3 | 22 | CH1 |
> | +18 | R3=20k | R4=2.21k | 25.12 | 10.05 | 45 | ADC4 | 24 | CH4 |
> | -18 | R6=20k | R5=2.21k | 30.12 | 12.05 | 44 | -ADC5 | 25 | CH3 |
> | +PAV | R7= 11.5k | R8=2.21k | 15.51 | 6.204 | 46 | ADC6 | 27 | CH6 |
> | -PAV | R10=11.5k | R9=2.21k | 18.4 | 7.35 | 5 | -ADC7 | 28 | CH7 |
> | +5 | R11=11.5k | R12=2.21k | 15.51 | 6.204 | 6 | ADC8 | 1 | CH8 |
> | +24 | R13=42.2k | R14=2.21k | 50.24 | 20.10 | 17 | ADC9 | 2 | CH9 |

Several corrections from the 6/19/15 version. The negative voltages are loaded with 10k from the inverters the quoted V for 2.5 and 1/Avs now reflect that. The pin and ADC inputs are now more correct.

> --
> Bruce Atwood PhD
> Department of Astronomy
> The Ohio State University
> 140 West 18th Ave.
> Columbus, OH 43210-1173
>
> Phone 614.292.6279
> FAX 614.292.2928

--
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Sang-Mok CHA

보낸 사람: "Bruce Atwood" <atwood.1@osu.edu>
날짜: 2016년 9월 6일 화요일 오후 12:43
받는 사람: "Daniel Pappalardo" <pappalardo.1@osu.edu>; "'Sang-Mok CHA'" <chasm@kasi.re.kr>; "Yongseok LEE" <yslee@kasi.re.kr>
참조: <atwood.1@osu.edu>
제목: Regulator boards

I have replaced C25 (was 2.2uF) with a 10uF Polymer Tantalum capacitor on the eight Regulator boards in Columbus, serial numbers:

09

11

20

4

2015-01

2015-02

2015-03

2015-04.

I have put a label over the silk screen "Rev B" which says Rev C. You will find, in the bag with the remainder of the capacitors, more Rev C labels.

--
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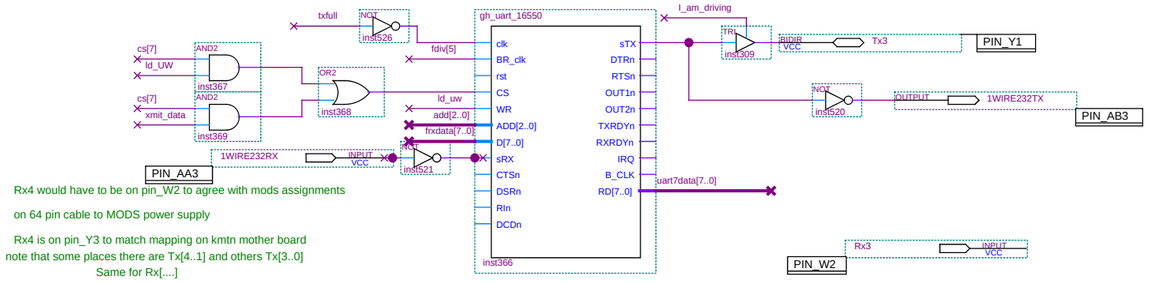
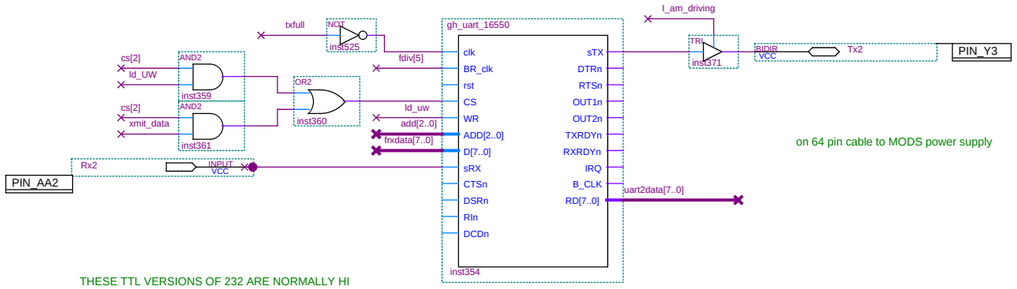
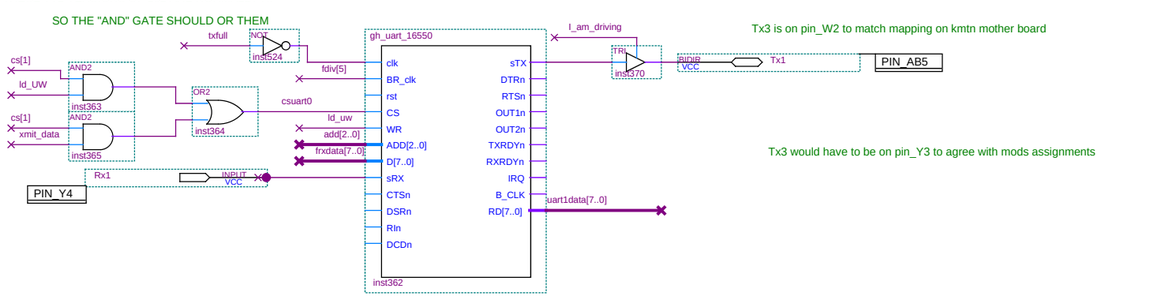
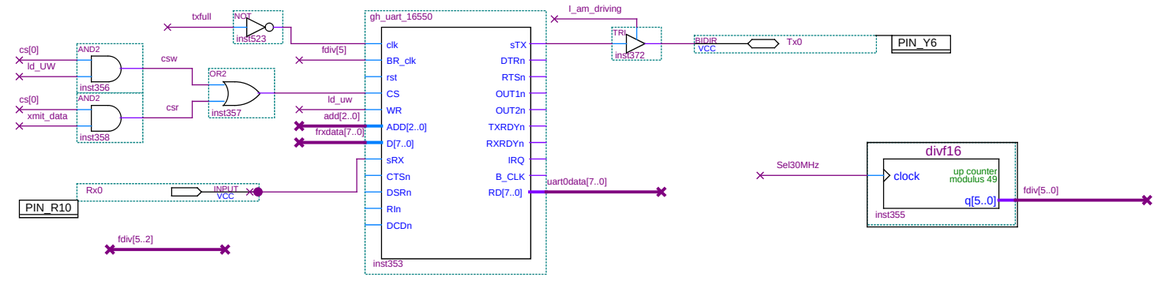
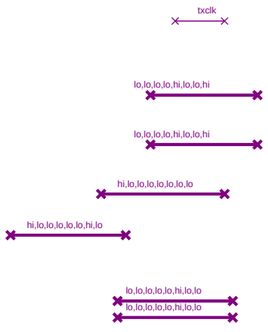

txfull
NOT
inst526
fdiv[5]
cs[7]
ld_UW
AND2
inst367
cs[7]
xmit_data
AND2
inst369
OR2
inst368
ld_uw
add[2..0]
frxdata[7..0]
1WIRE232RX
INPUT
VCC
NOT
inst521
PIN_AA3
gh_uart_16550
clk
BR_clk
rst
CS
WR
ADD[2..0]
D[7..0]
sRX
CTSn
DSRn
RIn
DCDn
sTX
DTRn
RTSn
OUT1n
OUT2n
TXRDYn
RXRDYn
IRQ
B_CLK
RD[7..0]
inst366
I_am_driving
TRI
inst309
BIDIR
VCC
Tx3
PIN_Y1
NOT
inst520
OUTPUT
1WIRE232TX
PIN_AB3
uart7data[7..0]
Rx4 would have to be on pin_W2 to agree with mods assignments
on 64 pin cable to MODS power supply
Rx4 is on pin_Y3 to match mapping on kmtn mother board
note that some places there are Tx[4..1] and others Tx[3..0]
Same for Rx[....]
Rx3
INPUT
VCC
PIN_W2


txfull
NOT
inst525
fdiv[5]
cs[2]
ld_UW
AND2
inst359
cs[2]
xmit_data
AND2
inst361
OR2
inst360
ld_uw
add[2..0]
frxdata[7..0]
Rx2
INPUT
VCC
PIN_AA2
gh_uart_16550
clk
BR_clk
rst
CS
WR
ADD[2..0]
D[7..0]
sRX
CTSn
DSRn
RIn
DCDn
sTX
DTRn
RTSn
OUT1n
OUT2n
TXRDYn
RXRDYn
IRQ
B_CLK
RD[7..0]
inst354
I_am_driving
TRI
inst371
BIDIR
VCC
Tx2
PIN_Y3
uart2data[7..0]
on 64 pin cable to MODS power supply
THESE TTL VERSIONS OF 232 ARE NORMALLY HI

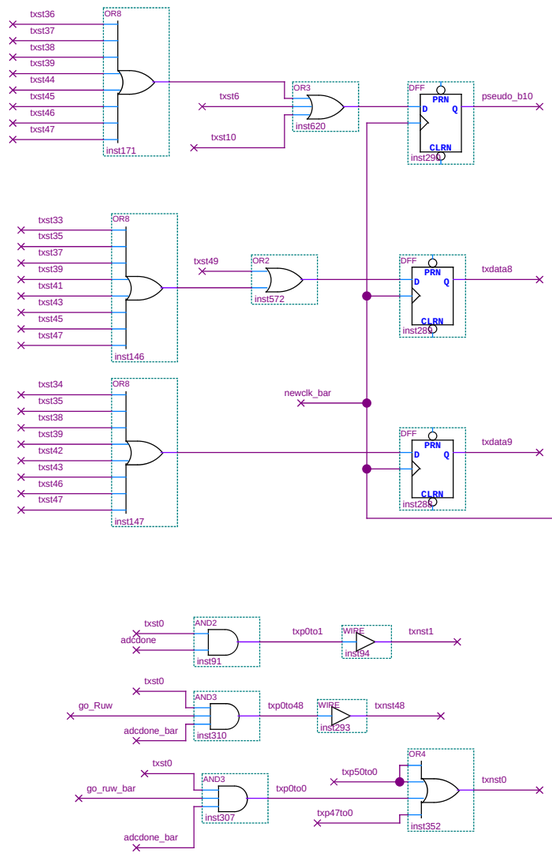

SO THE "AND" GATE SHOULD OR THEM
txfull
NOT
inst524
fdiv[5]
cs[1]
ld_UW
AND2
inst363
cs[1]
xmit_data
AND2
inst365
OR2
inst364
csuart0
ld_uw
add[2..0]
frxdata[7..0]
Rx1
INPUT
VCC
PIN_Y4
gh_uart_16550
clk
BR_clk
rst
CS
WR
ADD[2..0]
D[7..0]
sRX
CTSn
DSRn
RIn
DCDn
sTX
DTRn
RTSn
OUT1n
OUT2n
TXRDYn
RXRDYn
IRQ
B_CLK
RD[7..0]
inst362
I_am_driving
TRI
inst370
BIDIR
VCC
Tx1
PIN_AB5
uart1data[7..0]
Tx3 is on pin_W2 to match mapping on kmtn mother board
Tx3 would have to be on pin_Y3 to agree with mods assignments

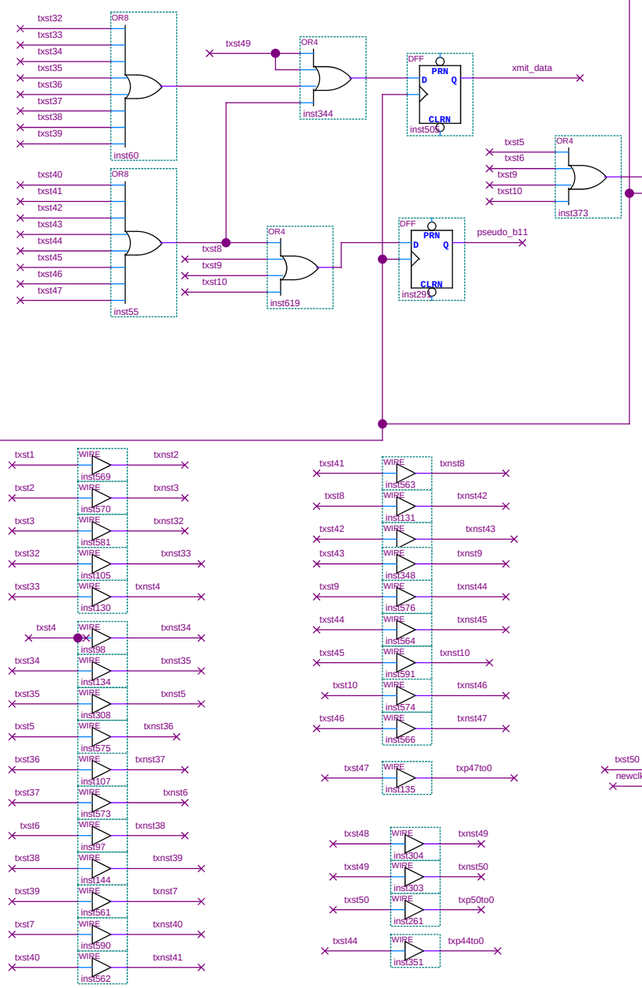

txfull
NOT
inst523
fdiv[5]
cs[0]
ld_UW
AND2
inst356
cs[0]
xmit_data
AND2
inst358
csw
csr
OR2
inst357
ld_uw
add[2..0]
frxdata[7..0]
Rx0
INPUT
VCC
PIN_R10
fdiv[5..2]
gh_uart_16550
clk
BR_clk
rst
CS
WR
ADD[2..0]
D[7..0]
sRX
CTSn
DSRn
RIn
DCDn
sTX
DTRn
RTSn
OUT1n
OUT2n
TXRDYn
RXRDYn
IRQ
B_CLK
RD[7..0]
inst353
I_am_driving
TRI
inst372
BIDIR
VCC
Tx0
PIN_Y6
uart0data[7..0]
Sel30MHz
divf16
clock
up counter
modulus 49
q[5..0]
inst355
fdiv[5..0]

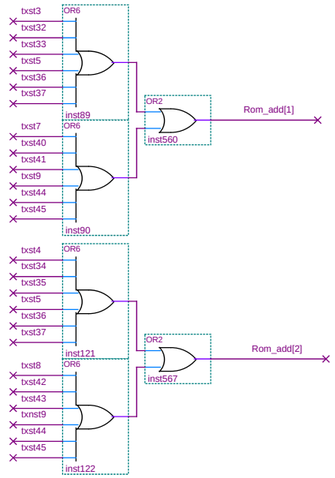
GND
NOT
inst2
HI
NOT
inst3
lo

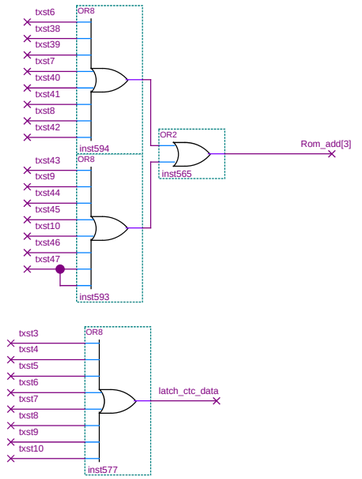

txclk
lo,lo,lo,lo,hi,lo,lo,hi
lo,lo,lo,lo,hi,lo,lo,hi
hi,lo,lo,lo,lo,lo,lo,lo
hi,lo,lo,lo,lo,lo,hi,lo
lo,lo,lo,lo,lo,hi,lo,lo
lo,lo,lo,lo,lo,hi,lo,lo

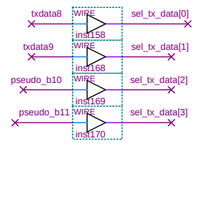
UARTS

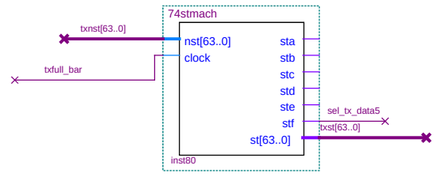


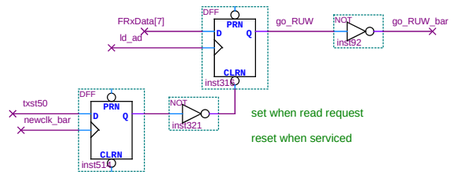




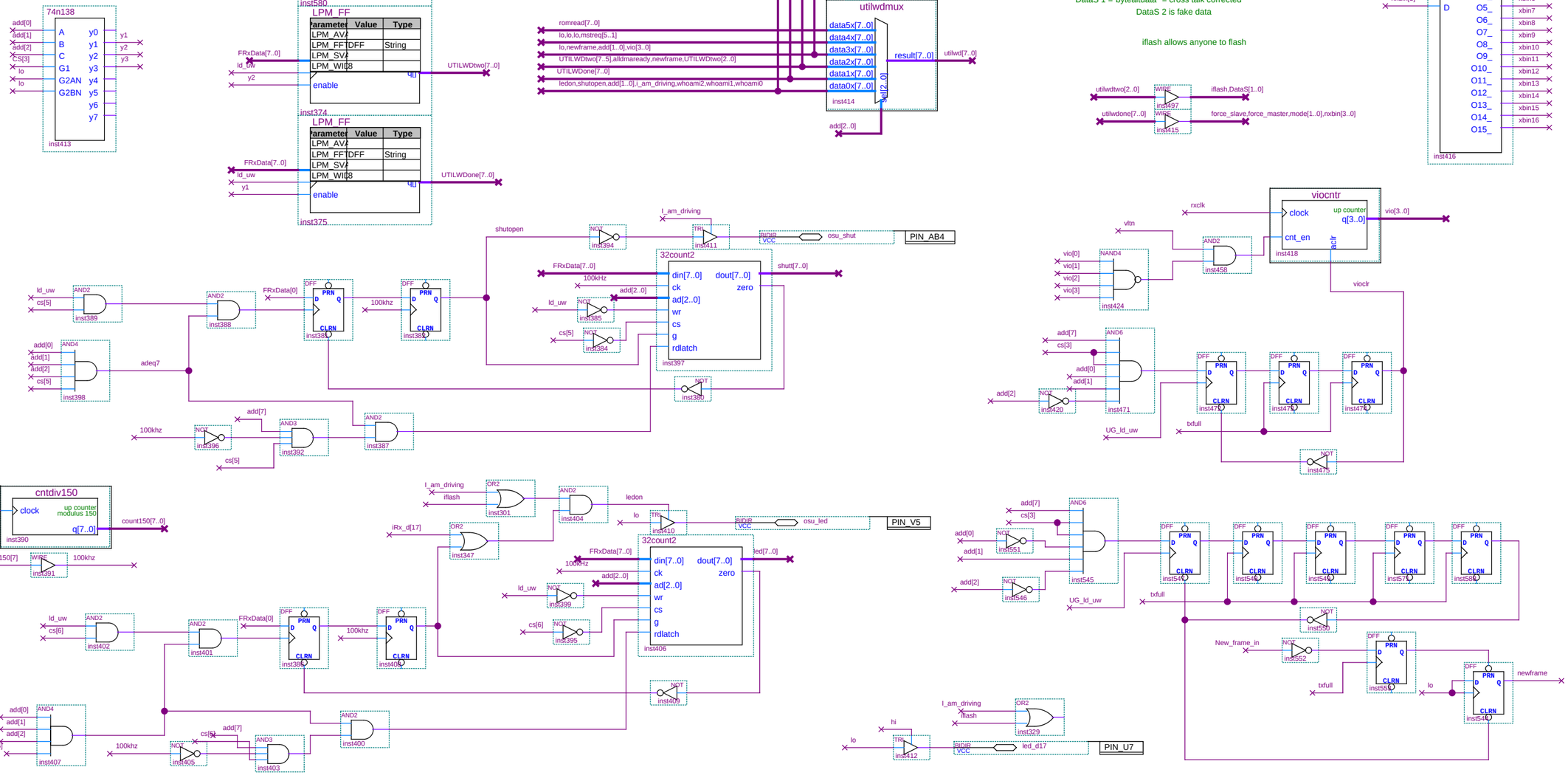






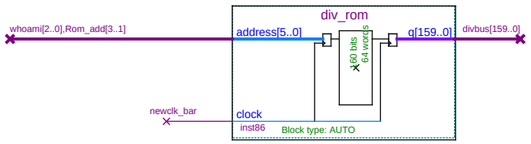


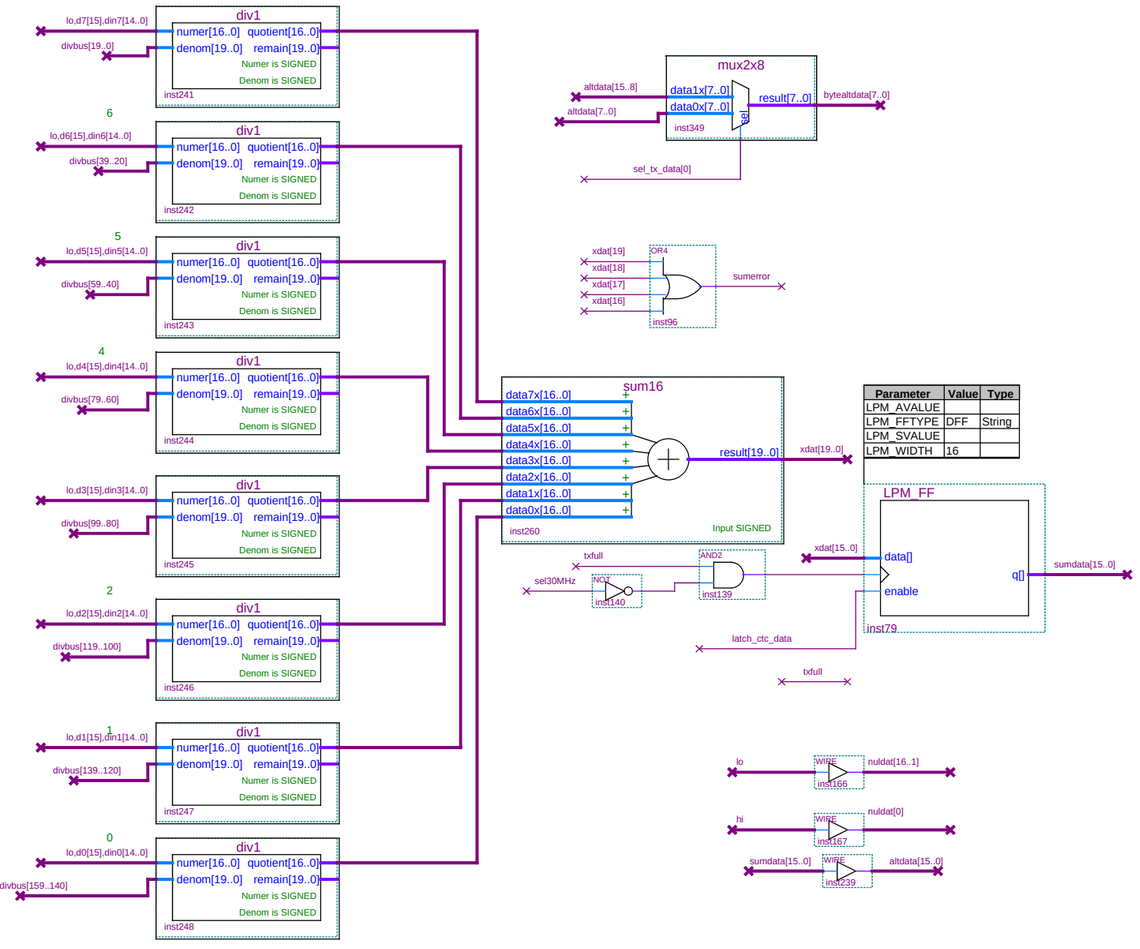
XMIT State Mach

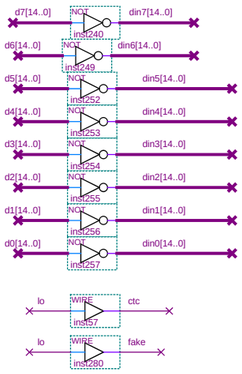


Shutter & LED Timers

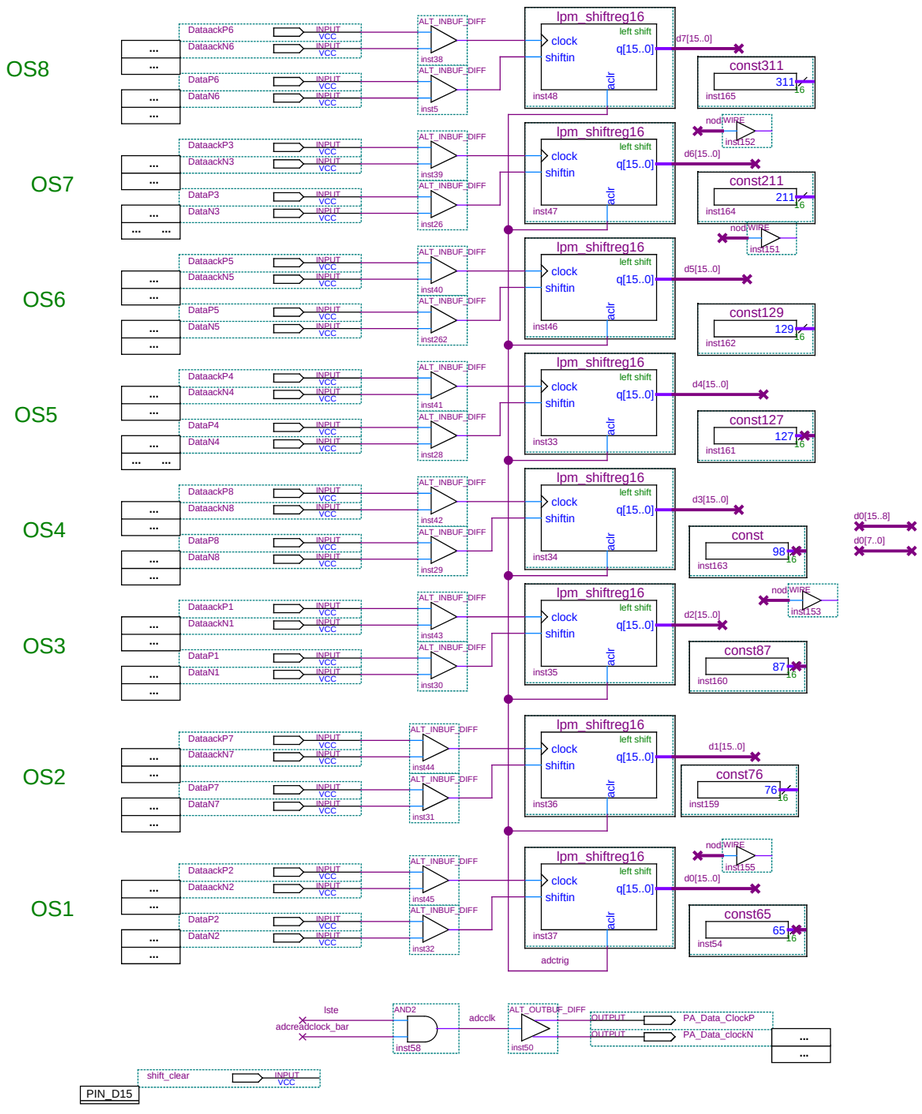
UW latch and readback

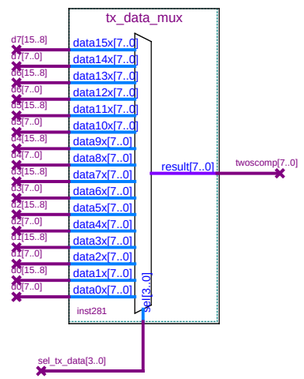




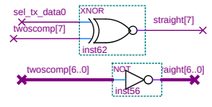


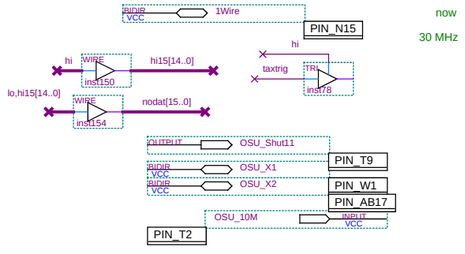
xtalk correction



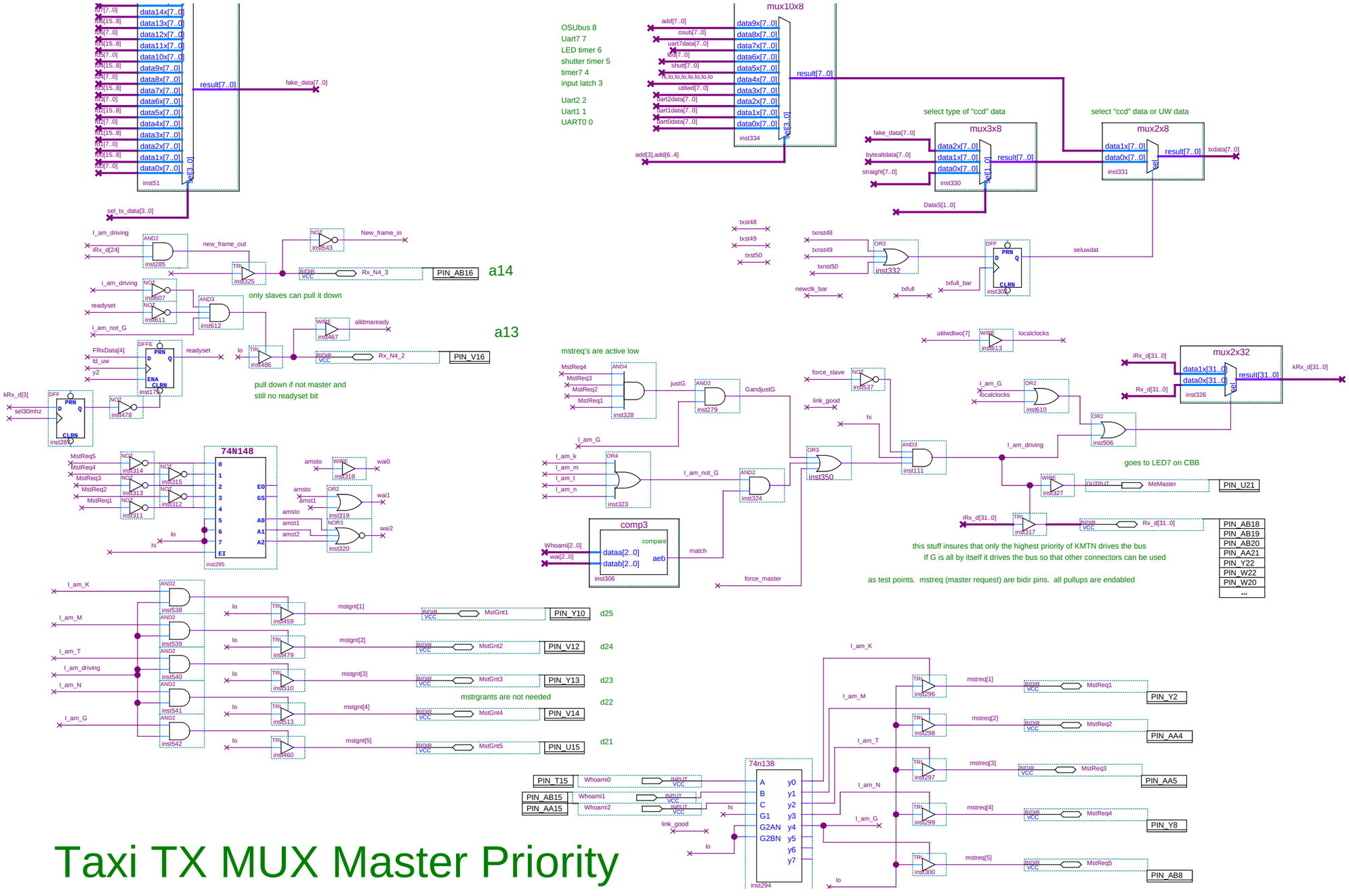


xor inverts MSB of 16 bit word to undo 2s comp

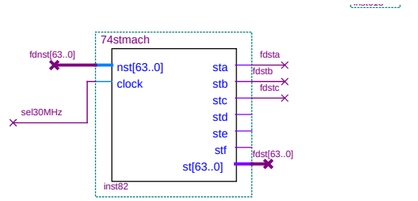


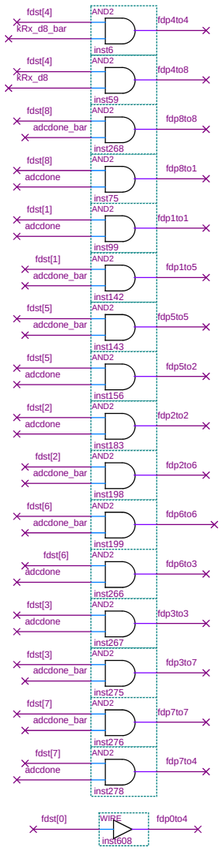


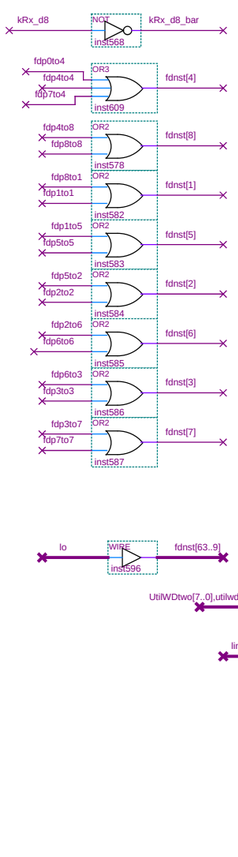
Data Sfift Reg and MUX

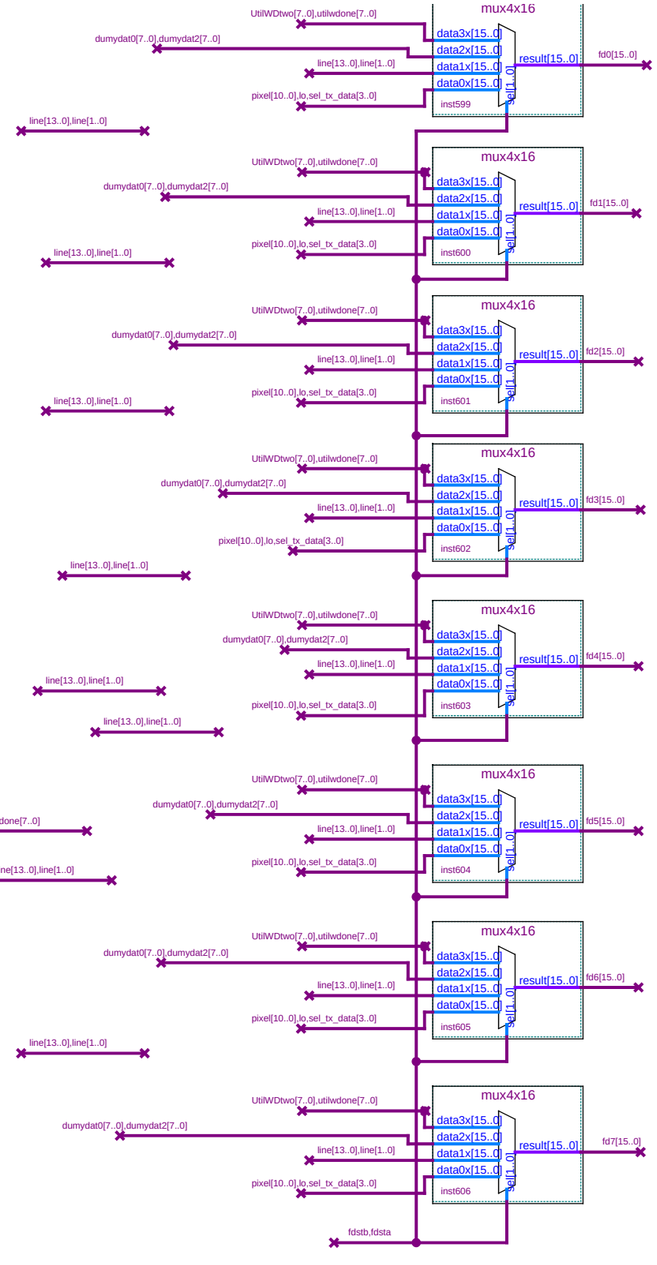


Taxi TX MUX Master Priority

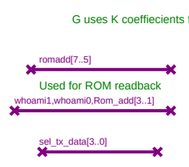


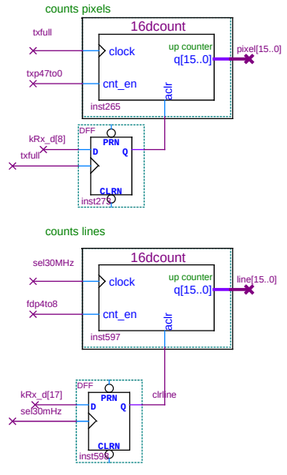


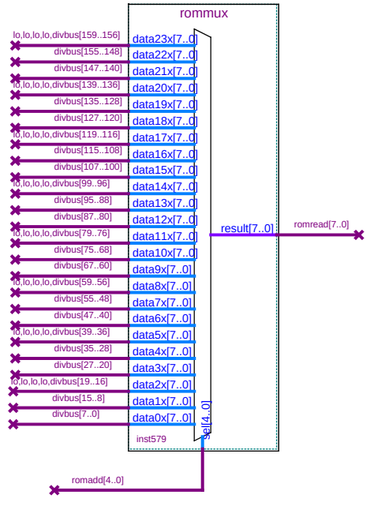




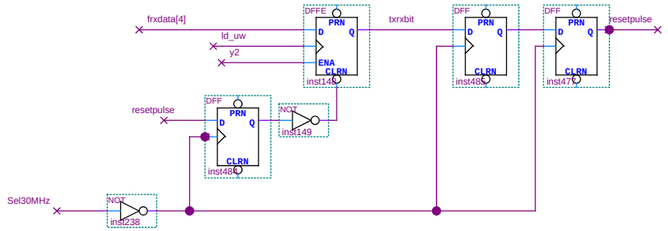
G uses K coeffiecients for now

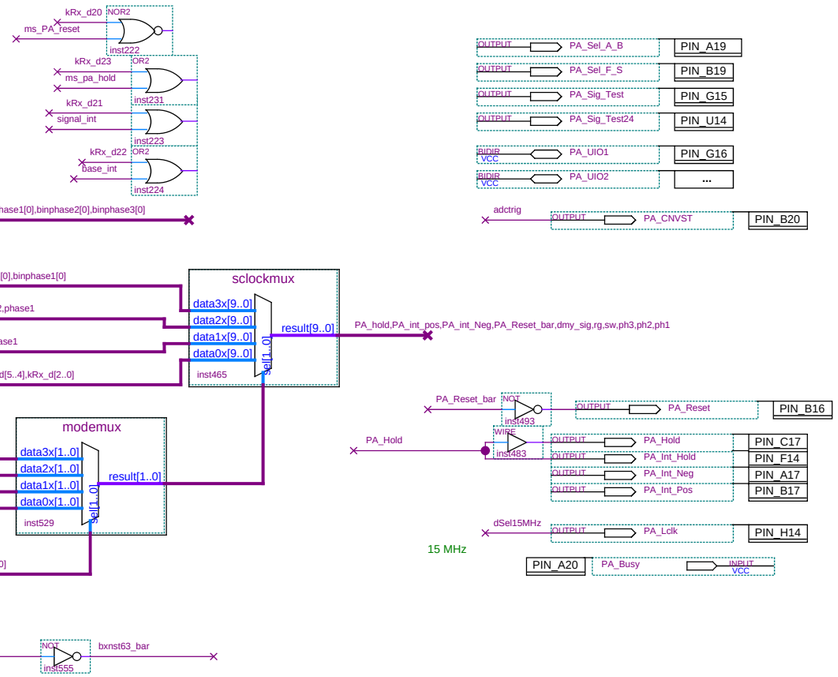




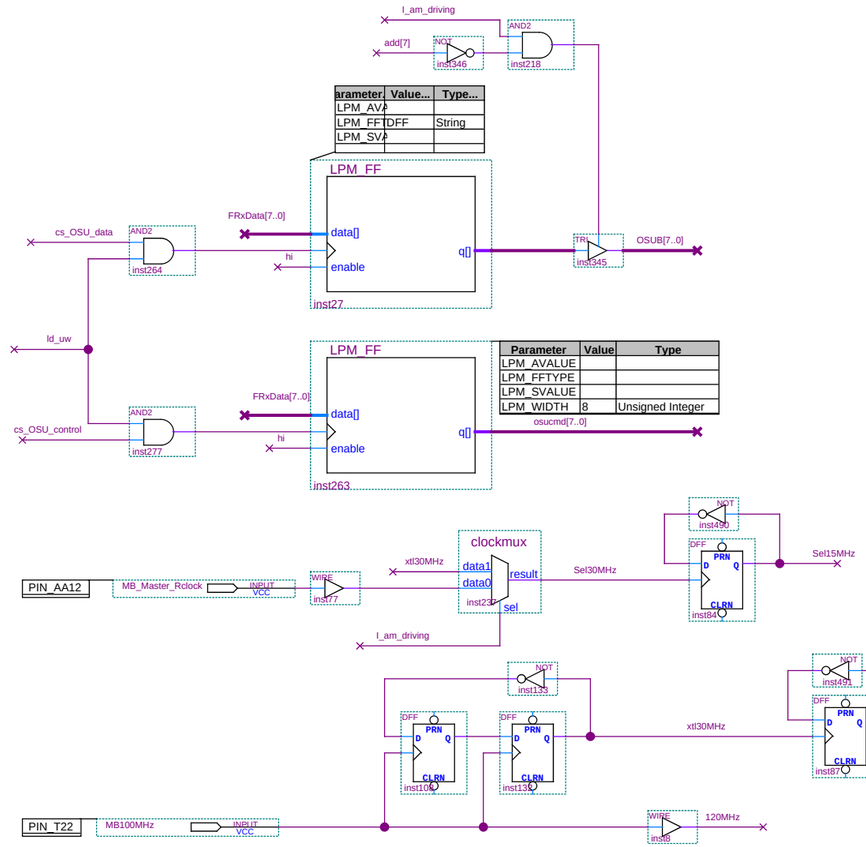


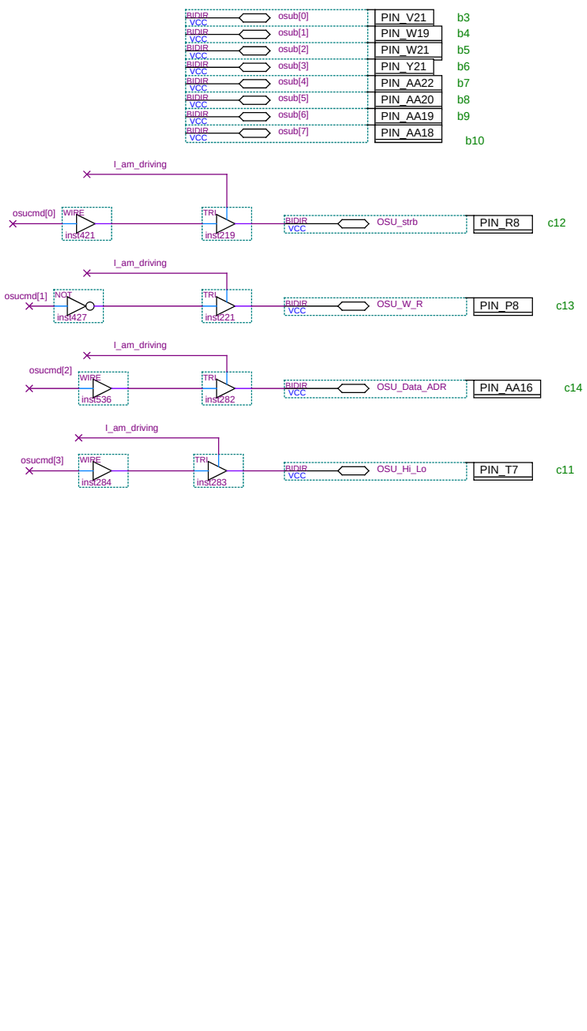
Dummy Data

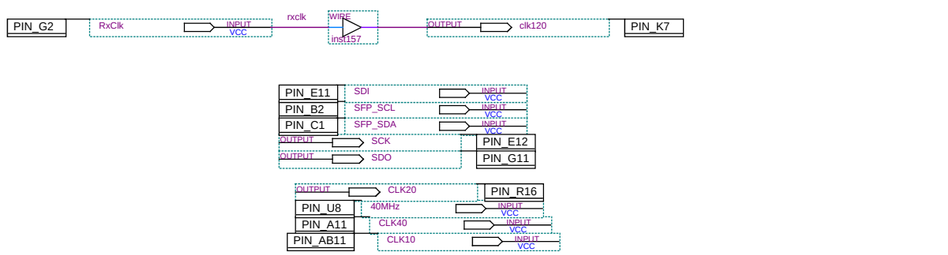

frxdata[4]
ld_uw
y2
DFFE
PRN
D
Q
ENA
CLRN
inst14
txrxbit
DFF
inst48
inst47
resetpulse
resetpulse
NOT
inst149
inst48
Sel30MHz
inst238


kRx_d20
NOR2
ms_PA_reset
inst222
kRx_d23
ms_pa_hold
inst231
kRx_d21
signal_int
inst223
kRx_d22
base_int
inst224
binphase1[0],binphase2[0],binphase3[0]
ms_pa_hold,base_int,signal_int,ms_pa_reset,lo,ms_CCD_reset,ms_sw_bar,binphase3[0],binphase2[0],binphase1[0]
ms_pa_hold,base_int,signal_int,ms_pa_reset,ms_dmy_sig,ms_CCD_reset,ms_sw_bar,phase3,phase2,phase1
Gpa_hold,Gbase_int,Gsig_int,GPA_reset,lo,G_CCD_reset,lo,gphase3,gphase2,gphase1
krx_d[23..20],seq_dmy_sig,kRx_d[5..4],kRx_d[2..0]
sclockmux
data3x[9..0]
data2x[9..0]
data1x[9..0]
data0x[9..0]
result[9..0]
sel[1..0]
inst465
PA_hold,PA_int_pos,PA_int_Neg,PA_Reset_bar,dmy_sig,rg,sw,ph3,ph2,ph1
modemux
kRx_d7,bxnst63_bar
lo,hi
lo,lo
kRx_d7,bxnst63_bar
data3x[1..0]
data2x[1..0]
data1x[1..0]
data0x[1..0]
result[1..0]
sel[1..0]
inst529
mode[1..0]
bxnst[63]
NOT
inst555
bxnst63_bar
OUTPUT
PA_Sel_A_B
PIN_A19
PA_Sel_F_S
PIN_B19
PA_Sig_Test
PIN_G15
PA_Sig_Test24
PIN_U14
BIDIR
VCC
PA_UIO1
PIN_G16
PA_UIO2
...
adctrig
PA_CNVST
PIN_B20
PA_Reset_bar
NOT
inst493
PA_Reset
PIN_B16
PA_Hold
WIRE
inst483
PA_Hold
PIN_C17
PA_Int_Hold
PIN_F14
PA_Int_Neg
PIN_A17
PA_Int_Pos
PIN_B17
dSel15MHz
PA_Lclk
PIN_H14
15 MHz
PIN_A20
PA_Busy
INPUT
VCC

d MUX modes

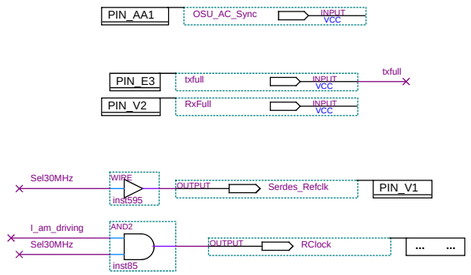

I_am_driving
add[7]
NOT
inst1346
AND2
inst218
LPM_FF
data[]
enable
q[]
inst27
cs_OSU_data
AND2
inst264
FRxData[7..0]
hi
TRI
inst1345
OSUB[7..0]
ld_uw
cs_OSU_control
inst277
inst263
Parameter Value Type
LPM_AVALUE
LPM_FFTYPE
LPM_SVALUE
LPM_WIDTH 8 Unsigned Integer
osucmd[7..0]
clockmux
data1
data0
sel
result
inst233
xtl30MHz
Sel30MHz
Sel15MHz
DFF
PRN
CLRN
inst840
inst430
PIN_AA12
MB_Master_Rclock
INPUT
VCC
WIRE
inst77
inst1100
inst1156
inst491
inst873
Xtl15MHz
PIN_T22
MB100MHz
inst48
120MHz

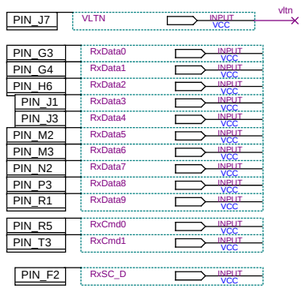

PIN_V21 b3
PIN_W19 b4
PIN_W21 b5
PIN_Y21 b6
PIN_AA22 b7
PIN_AA20 b8
PIN_AA19 b9
PIN_AA18 b10
osub[0]
osub[1]
osub[2]
osub[3]
osub[4]
osub[5]
osub[6]
osub[7]
BIDIR
VCC
I_am_driving
osucmd[0]
osucmd[1]
osucmd[2]
osucmd[3]
WIRE
TRI
inst421
inst219
OSU_strb
PIN_R8 c12
inst427
inst221
OSU_W_R
PIN_P8 c13
inst536
inst282
OSU_Data_ADR
PIN_AA16 c14
inst284
inst283
OSU_Hi_Lo
PIN_T7 c11

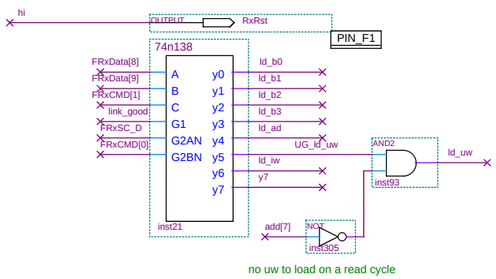

PIN_G2
RxClk
INPUT
VCC
rxclk
WIRE
inst157
OUTPUT
clk120
PIN_K7
PIN_E11 SDI
PIN_B2 SFP_SCL
PIN_C1 SFP_SDA
SCK
SDO
PIN_E12
PIN_G11
PIN_R16
CLK20
PIN_U8 40MHz
PIN_A11 CLK40
PIN_AB11 CLK10

hi
WIRE
inst480
pll2locked
inst492
pllllocked

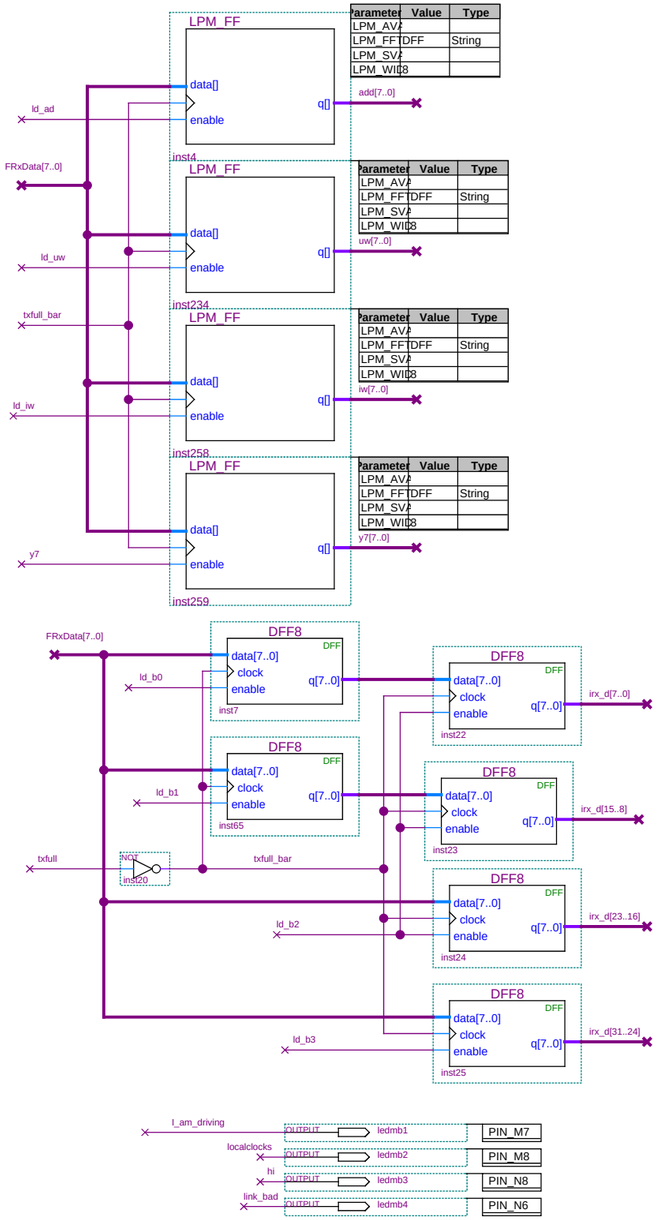
OSU Bus, PLL





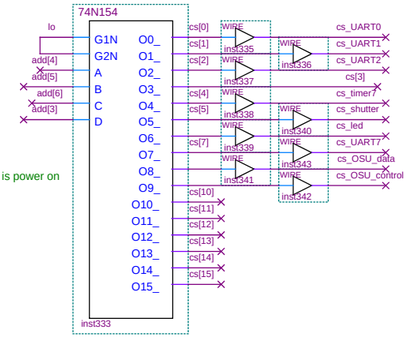


no uw to load on a read cycle

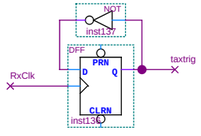


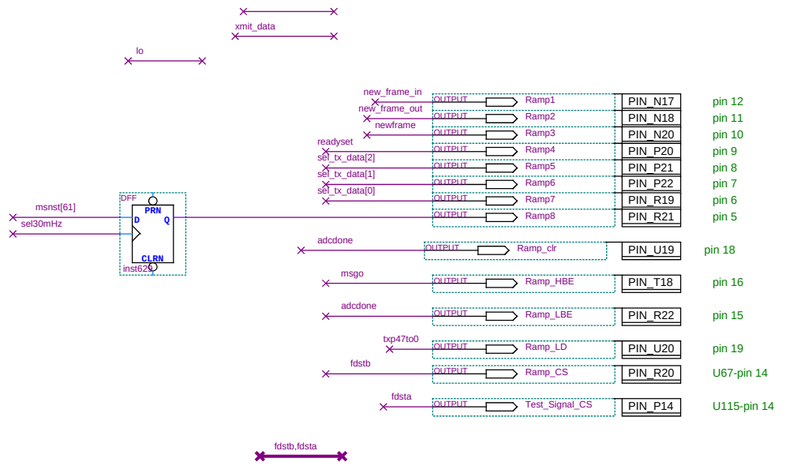
add3 as msb of CS is to match legacy Rx board

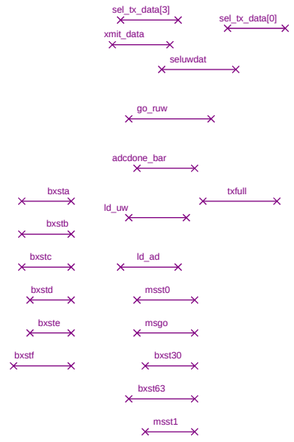
led 3 is power on

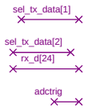


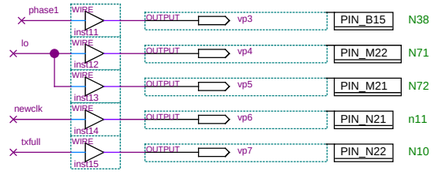
PCI d latch, add, uw,y7 CS generation



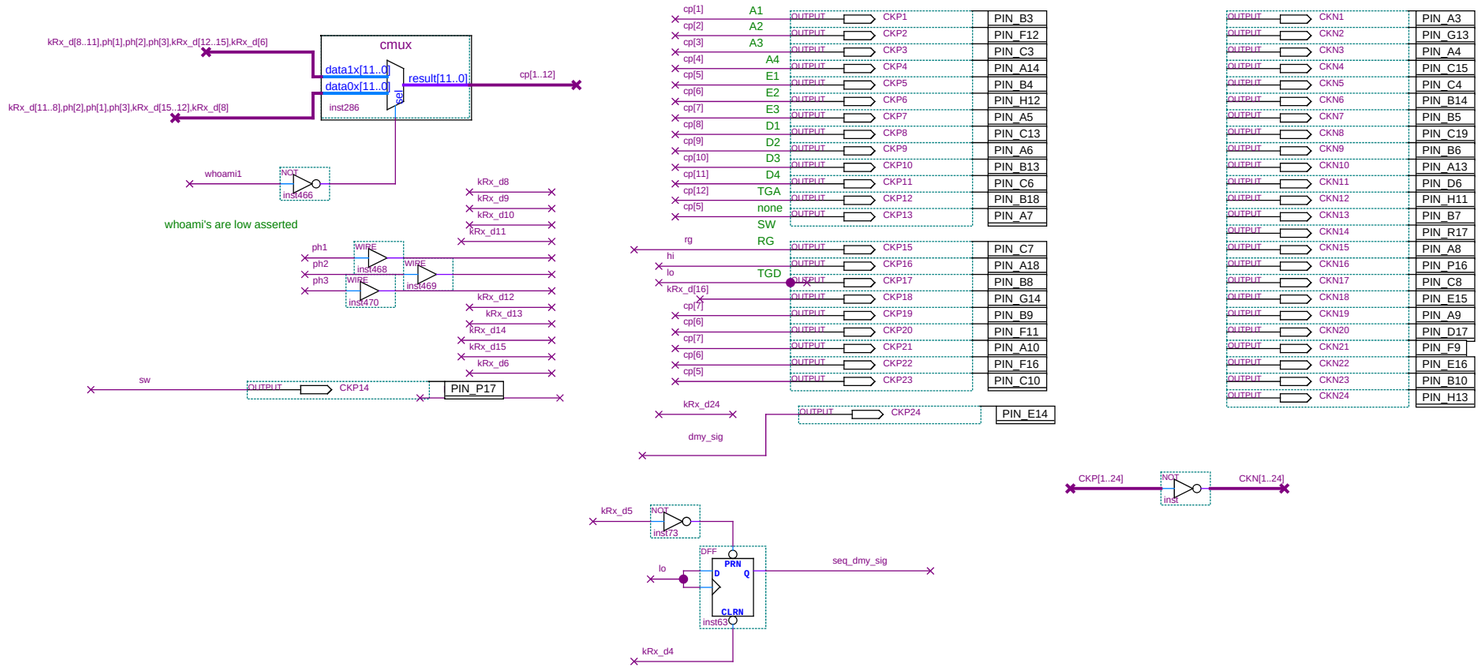




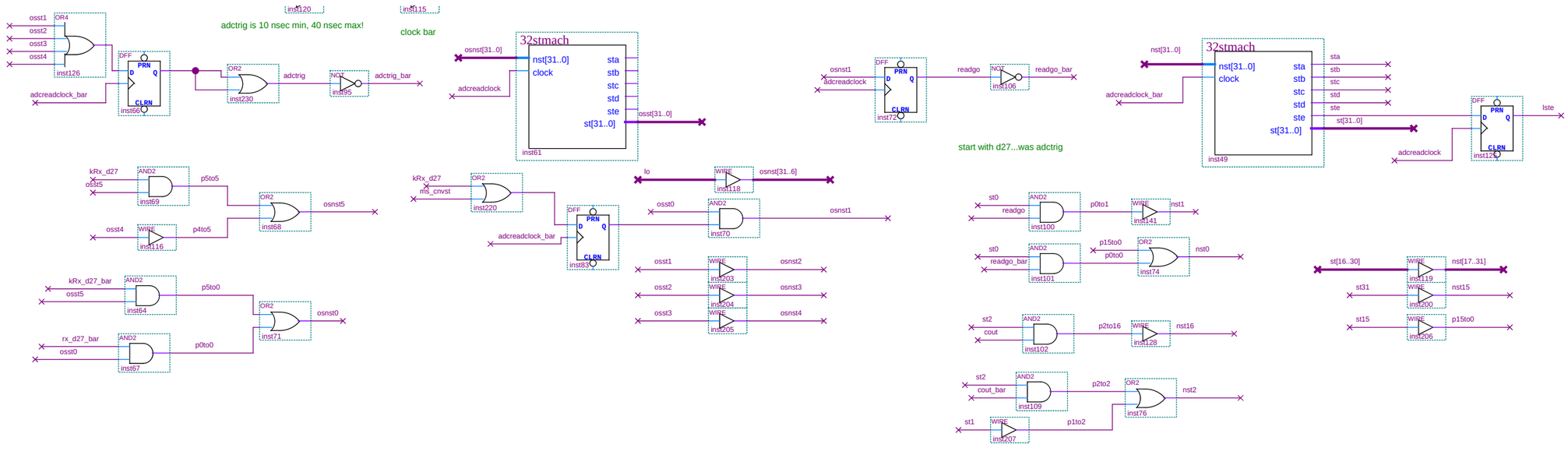


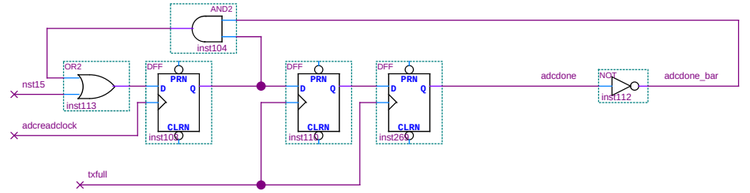


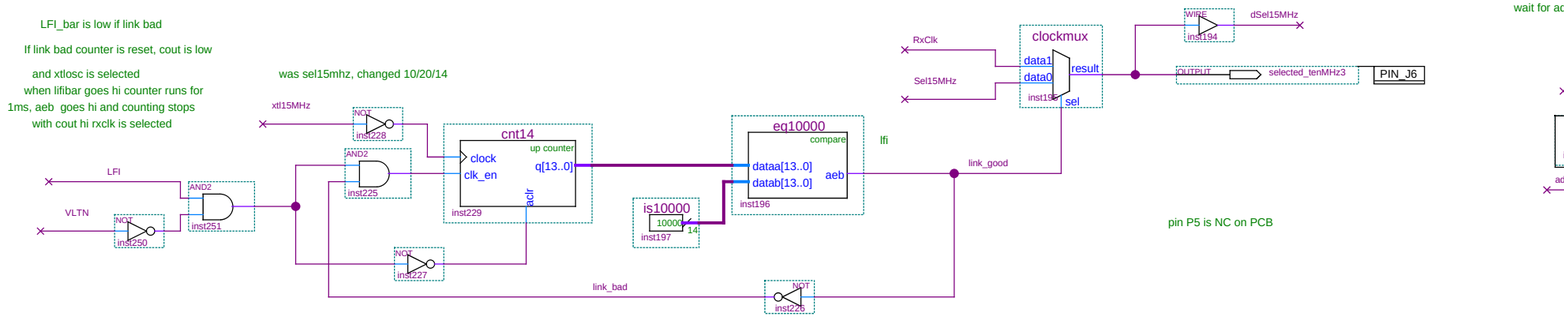
test points, Ramp, MStGnt



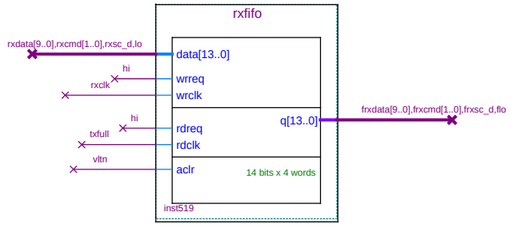
outputs to swiches

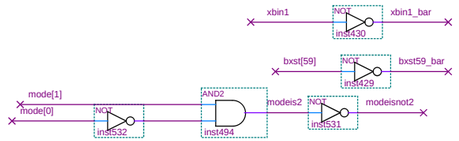


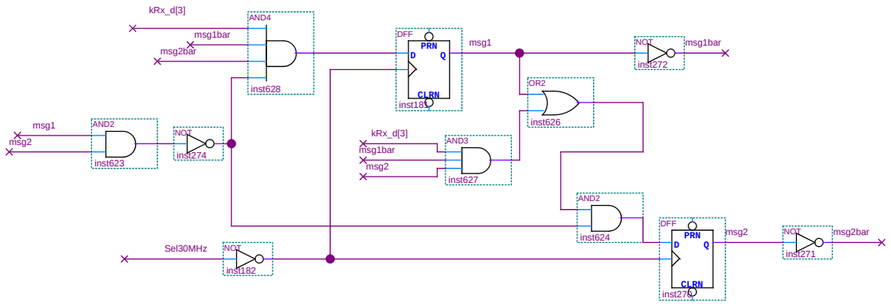


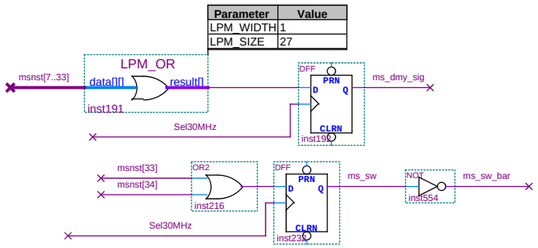


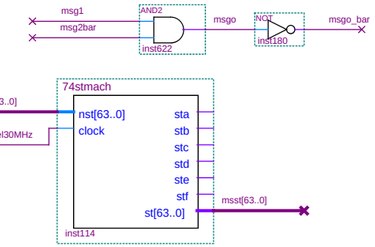
Link good, Sel 15MHz, ADC timing

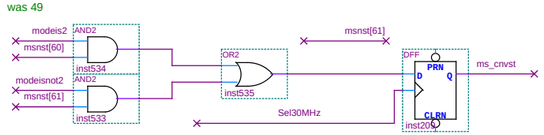


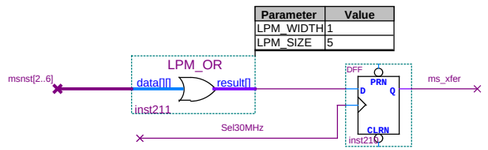


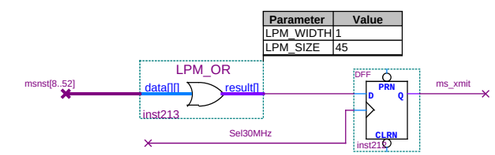


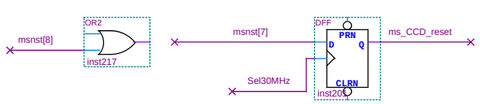


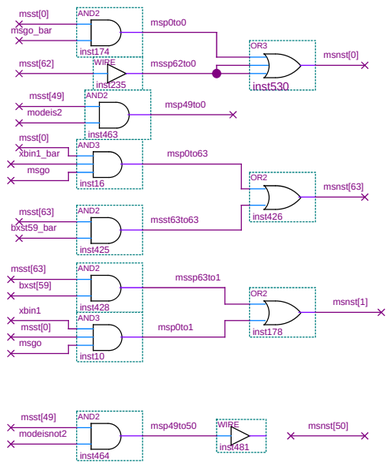




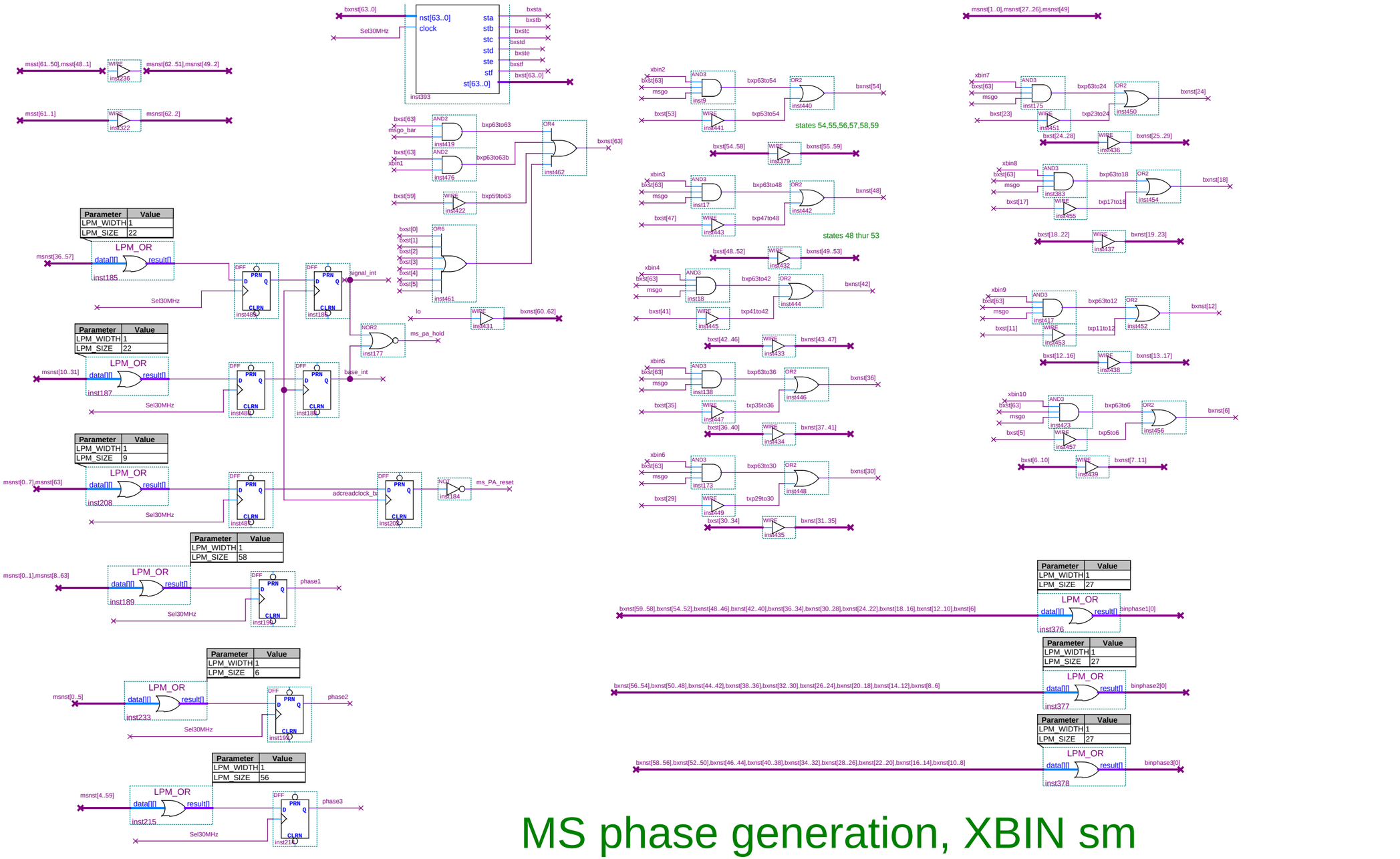








Rx FIFO, MS State Mach.



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LPM_SIZE	22

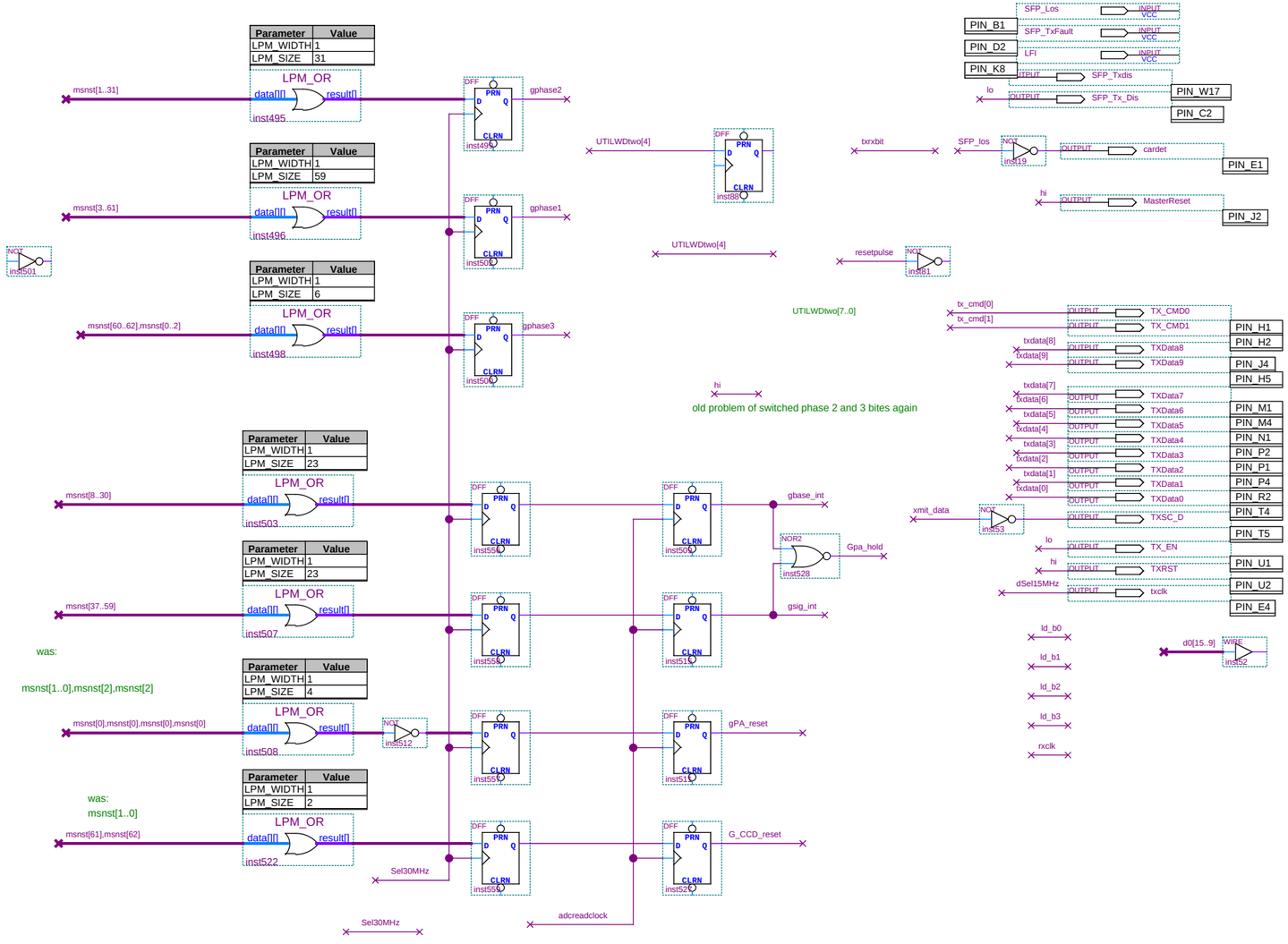
Parameter	Value
LPM_WIDTH	1
LPM_SIZE	9

Parameter	Value
LPM_WIDTH	1
LPM_SIZE	58

Parameter	Value
LPM_WIDTH	1
LPM_SIZE	6

Parameter	Value
LPM_WIDTH	1
LPM_SIZE	27

MS phase generation, XBIN sm



Guide Phase Generation

TITLE	KMTN CBB BGA part
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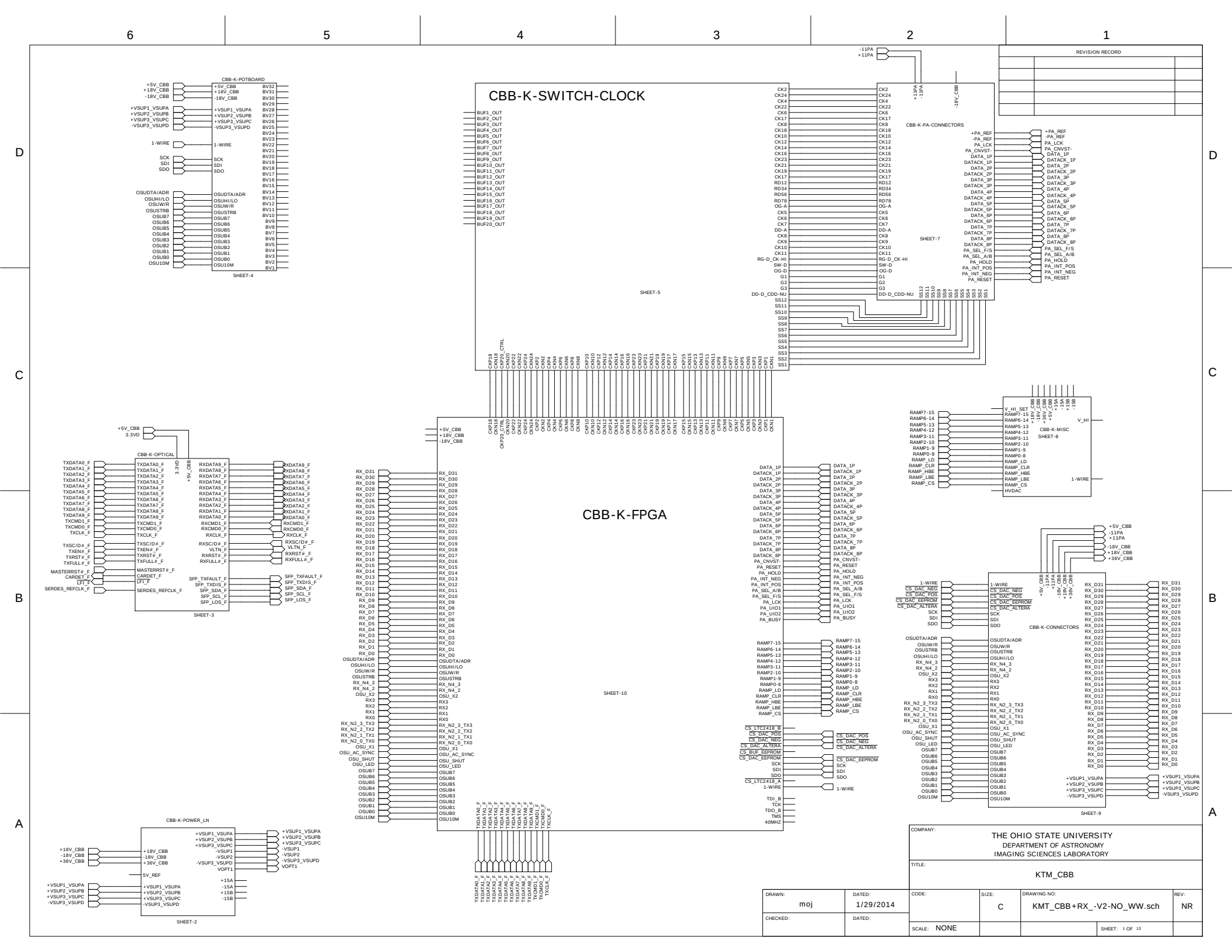
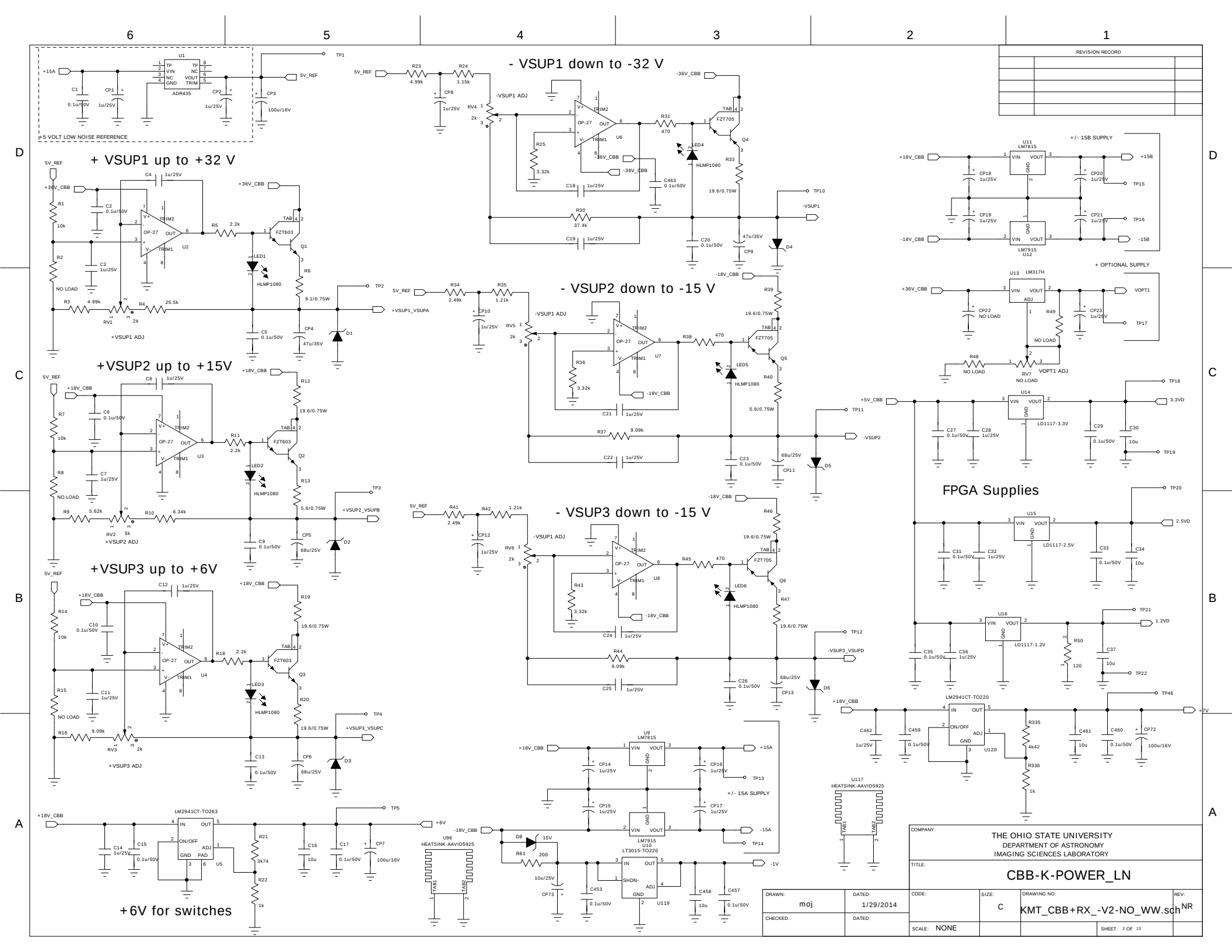
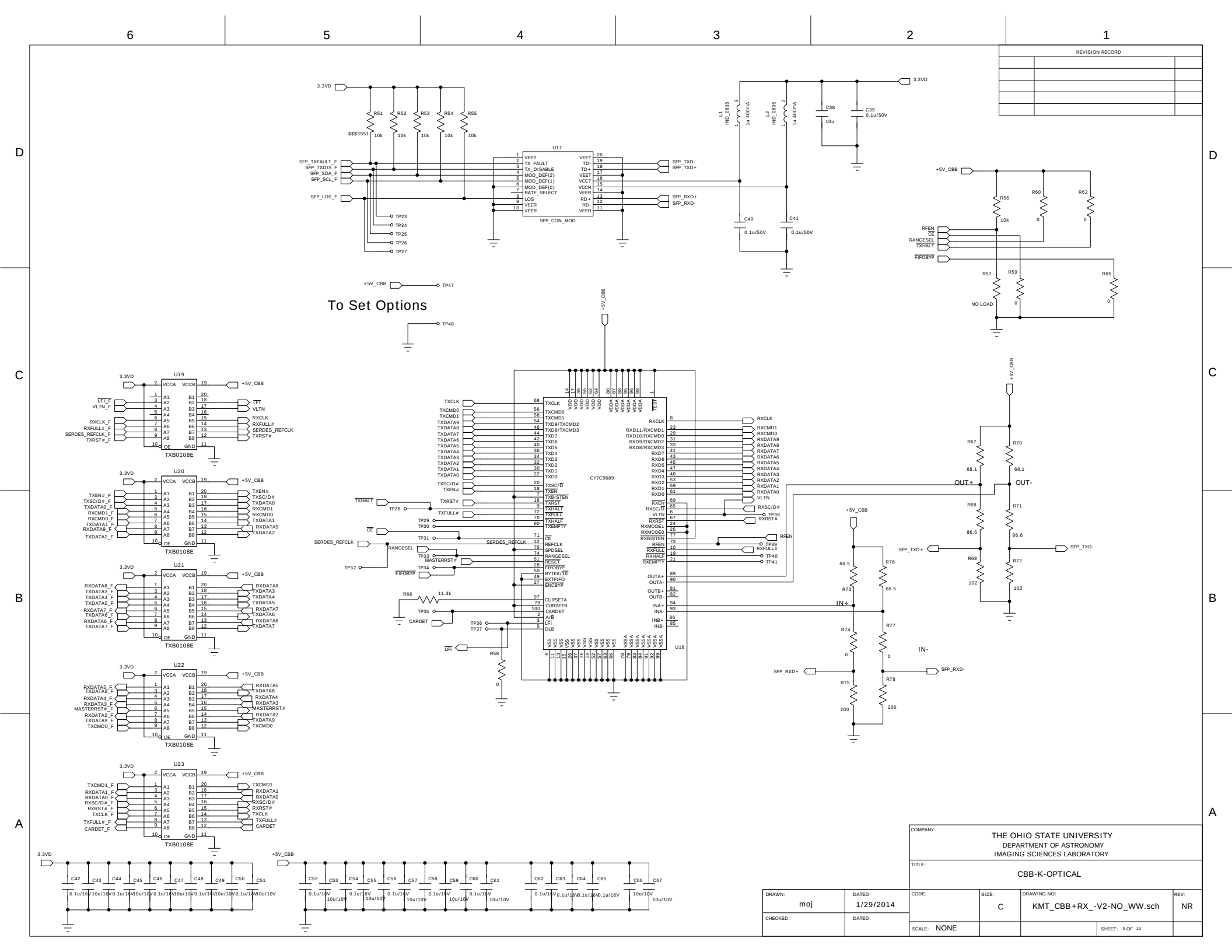
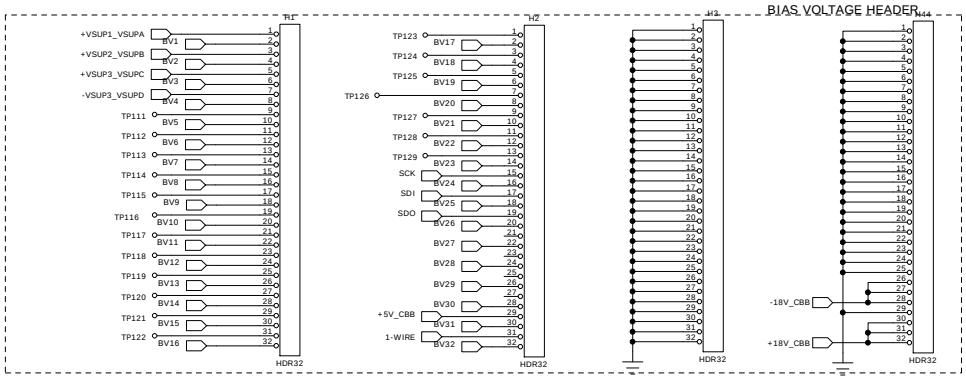
DESIGNER	atwood
NUMBER	1.00
REV	A
DATE	Tue Jun 16 13:46:29 2015
SHEET	1 OF 1


CBB-K-SWITCH-CLOCK
CBB-K-FPGA
CBB-K-POTBOARD
CBB-K-OPTICAL
CBB-K-POWER_LN
CBB-K-PA-CONNECTORS
CBB-K-MISC
CBB-K-CONNECTORS
SHEET-2
SHEET-3
SHEET-4
SHEET-5
SHEET-7
SHEET-8
SHEET-9
SHEET-10
REVISION RECORD
COMPANY:
THE OHIO STATE UNIVERSITY
DEPARTMENT OF ASTRONOMY
IMAGING SCIENCES LABORATORY
TITLE:
KTM_CBB
DRAWN:
moj
DATED:
1/29/2014
CHECKED:
DATED:
CODE:
SIZE:
C
DRAWING NO:
KMT_CBB+RX_-V2-NO_WW.sch
REV:
NR
SCALE:
NONE
SHEET:
1 OF 13

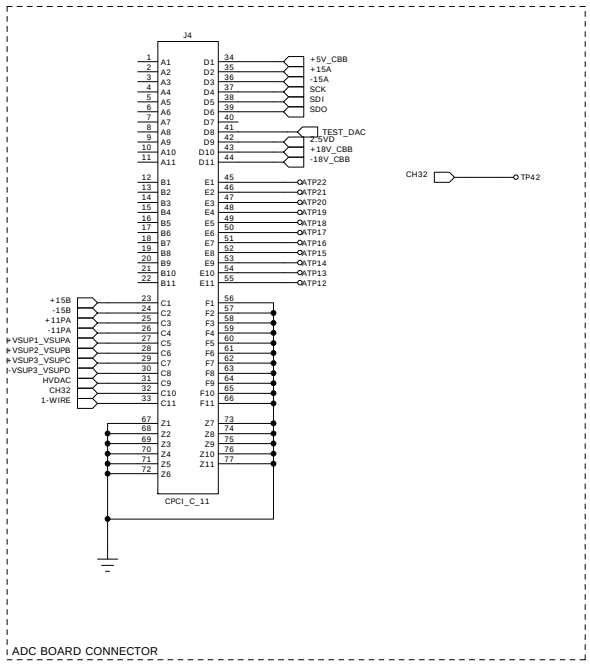

+5 VOLT LOW NOISE REFERENCE
ADR435
+15A
5V_REF
TP1
+ VSUP1 up to +32 V
+VSUP1 ADJ
HLMP1080
FZT603
OP-27
+VSUP1_VSUPA
TP2
+VSUP2 up to +15V
+VSUP2 ADJ
+VSUP2_VSUPB
TP3
+VSUP3 up to +6V
+VSUP3 ADJ
+VSUP3_VSUPC
TP4
+6V for switches
LM2941CT-TO263
TP5
+6V
- VSUP1 down to -32 V
-VSUP1 ADJ
-36V_CBB
FZT705
HLMP1080
-VSUP1
TP10
- VSUP2 down to -15 V
-VSUP2
TP11
- VSUP3 down to -15 V
-VSUP3_VSUPD
TP12
+/- 15A SUPPLY
LM7815
LM7915
LT3015-TO220
+15A
-15A
-1V
TP13
TP14
+/- 15B SUPPLY
+15B
-15B
TP15
TP16
+ OPTIONAL SUPPLY
LM317H
VOPT1
VOPT1 ADJ
TP17
FPGA Supplies
LD1117-3.3V
3.3VD
TP18
TP19
LD1117-2.5V
2.5VD
TP20
LD1117-1.2V
1.2VD
TP21
TP22
LM2941CT-TO220
+7V
TP46
HEATSINK-AAVID5925
REVISION RECORD
COMPANY:
THE OHIO STATE UNIVERSITY
DEPARTMENT OF ASTRONOMY
IMAGING SCIENCES LABORATORY
TITLE:
CBB-K-POWER_LN
DRAWN:
moj
DATED:
1/29/2014
CHECKED:
CODE:
SIZE:
C
DRAWING NO:
KMT_CBB+RX_-V2-NO_WW.sch
REV:
NR
SCALE:
NONE
SHEET:
2 OF 13


REVISION RECORD
To Set Options
U17
SFP_CON_MOD
U18
CY7C9689
U19
U20
U21
U22
U23
TXB0108E
THE OHIO STATE UNIVERSITY
DEPARTMENT OF ASTRONOMY
IMAGING SCIENCES LABORATORY
CBB-K-OPTICAL
DRAWN: moj
DATED: 1/29/2014
CHECKED:
CODE:
SIZE: C
DRAWING NO: KMT_CBB+RX_-V2-NO_WW.sch
REV: NR
SCALE: NONE
SHEET: 3 OF 13

REVISION RECORD		

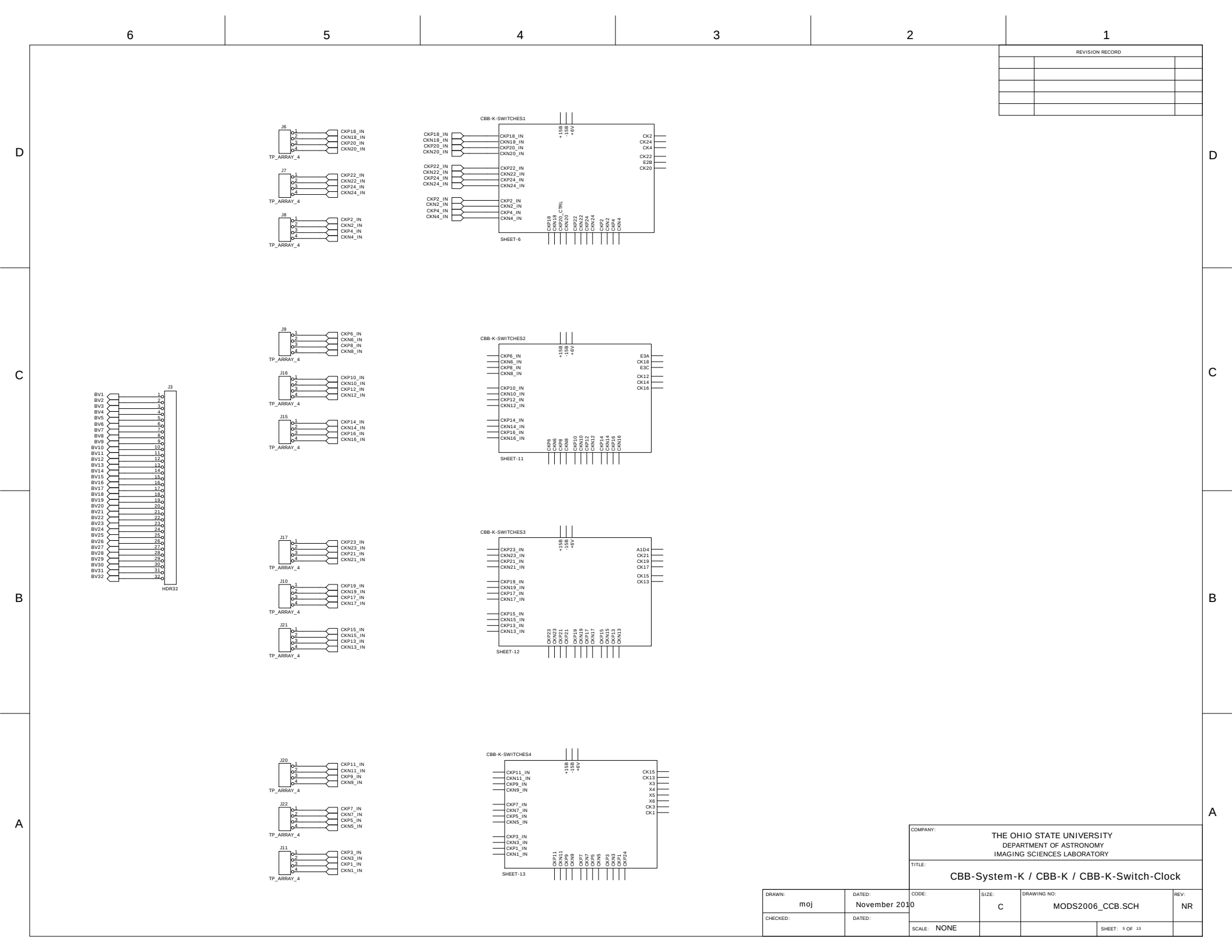


POT/DAC_BOARD_CONNECTOR



ADC BOARD CONNECTOR

COMPANY: THE OHIO STATE UNIVERSITY DEPARTMENT OF ASTRONOMY IMAGING SCIENCES LABORATORY						
TITLE: CBB-K-POTBOARD						
DRAWN: moj	DATED: 1/29/2014	CODE:	SIZE: C	DRAWING NO: KMT_CBB+RX_-V2-NO_WW.sch	REV: NR	
CHECKED:	DATED:	SCALE: NONE		SHEET: 4 OF 13		


6
5
4
3
2
1
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CKN18_IN
CKP20_IN
CKN20_IN
TP_ARRAY_4
J7
CKP22_IN
CKN22_IN
CKP24_IN
CKN24_IN
TP_ARRAY_4
J8
CKP2_IN
CKN2_IN
CKP4_IN
CKN4_IN
TP_ARRAY_4
CBB-K-SWITCHES1
CKP18_IN
CKN18_IN
CKP20_IN
CKN20_IN
CKP22_IN
CKN22_IN
CKP24_IN
CKN24_IN
CKP2_IN
CKN2_IN
CKP4_IN
CKN4_IN
+15B
-15B
+6V
CK2
CK24
CK4
CK22
E2B
CK20
CKP18
CKN18
CKP20_CTRL
CKN20
CKP22
CKN22
CKP24
CKN24
CKP2
CKN2
CKP4
CKN4
SHEET-6
J9
CKP6_IN
CKN6_IN
CKP8_IN
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J16
CKP10_IN
CKN10_IN
CKP12_IN
CKN12_IN
TP_ARRAY_4
J15
CKP14_IN
CKN14_IN
CKP16_IN
CKN16_IN
TP_ARRAY_4
CBB-K-SWITCHES2
CKP6_IN
CKN6_IN
CKP8_IN
CKN8_IN
CKP10_IN
CKN10_IN
CKP12_IN
CKN12_IN
CKP14_IN
CKN14_IN
CKP16_IN
CKN16_IN
+15B
-15B
+6V
E3A
CK18
E3C
CK12
CK14
CK16
CKP6
CKN6
CKP8
CKN8
CKP10
CKN10
CKP12
CKN12
CKP14
CKN14
CKP16
CKN16
SHEET-11
J3
BV1
BV2
BV3
BV4
BV5
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BV22
BV23
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BV25
BV26
BV27
BV28
BV29
BV30
BV31
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J10
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TP_ARRAY_4
J21
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CKP13_IN
CKN13_IN
TP_ARRAY_4
CBB-K-SWITCHES3
CKP23_IN
CKN23_IN
CKP21_IN
CKN21_IN
CKP19_IN
CKN19_IN
CKP17_IN
CKN17_IN
CKP15_IN
CKN15_IN
CKP13_IN
CKN13_IN
+15B
-15B
+6V
A1D4
CK21
CK19
CK17
CK15
CK13
CKP23
CKN23
CKP21
CKP19
CKN19
CKP17
CKN17
CKP15
CKN15
CKP13
CKN13
SHEET-12
J20
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J22
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CKP5_IN
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TP_ARRAY_4
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CKP1_IN
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+15B
-15B
+6V
CK15
CK13
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CKP7
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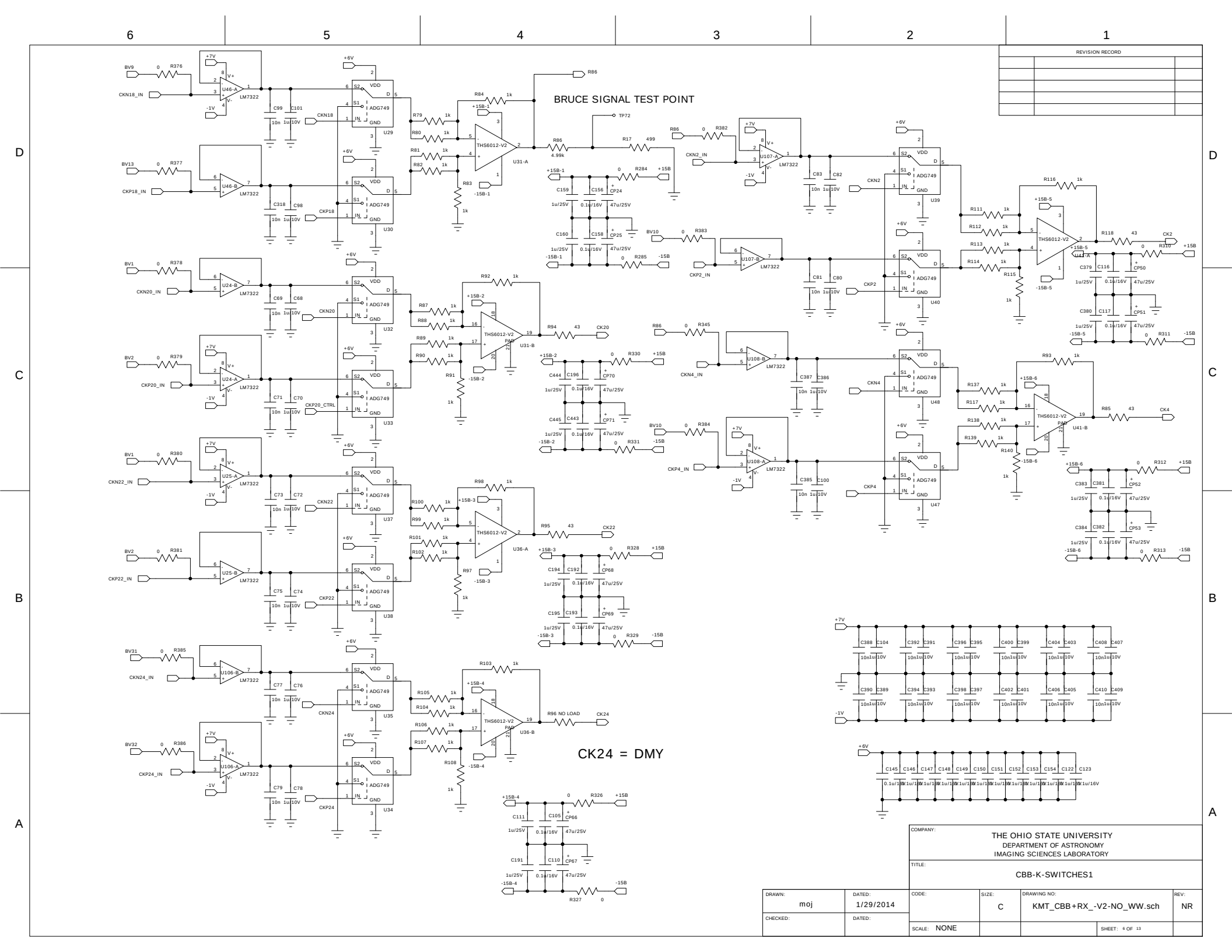
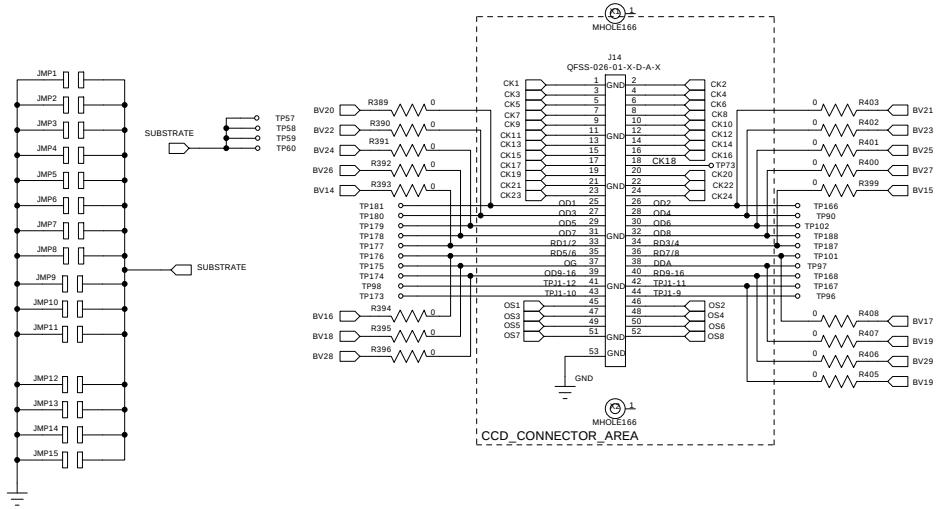
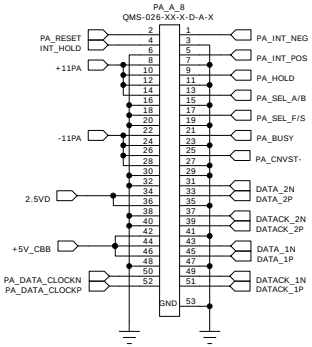
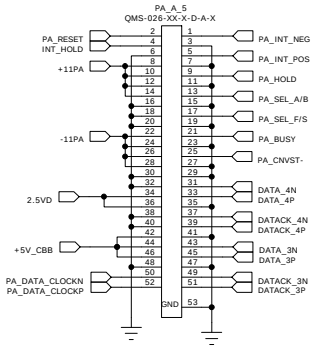
CKN5
CKP3
CKN3
CKP1
CKN1
CKP24
SHEET-13
COMPANY:
THE OHIO STATE UNIVERSITY
DEPARTMENT OF ASTRONOMY
IMAGING SCIENCES LABORATORY
TITLE:
CBB-System-K / CBB-K / CBB-K-Switch-Clock
DRAWN:
moj
DATED:
November 2010
CODE:
SIZE:
C
DRAWING NO:
MODS2006_CCB.SCH
REV:
NR
CHECKED:
DATED:
SCALE:
NONE
SHEET:
5 OF 13
D
C
B
A

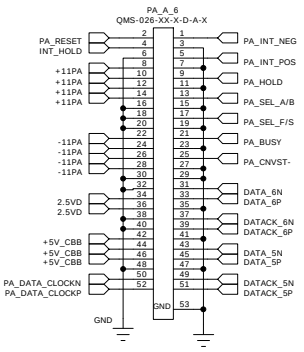

BRUCE SIGNAL TEST POINT
CK24 = DMY
REVISION RECORD
THE OHIO STATE UNIVERSITY
DEPARTMENT OF ASTRONOMY
IMAGING SCIENCES LABORATORY
CBB-K-SWITCHES1
DRAWN: moj
DATED: 1/29/2014
CHECKED:
CODE:
SIZE: C
DRAWING NO: KMT_CBB+RX_-V2-NO_WW.sch
REV: NR
SCALE: NONE
SHEET: 6 OF 13

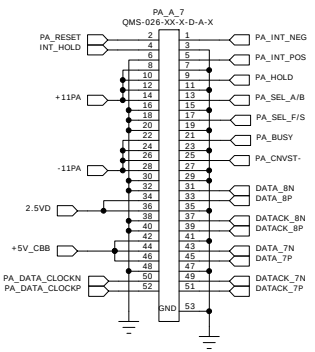
REVISION RECORD		
	reversed CCD connector	3/1/13

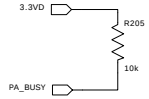


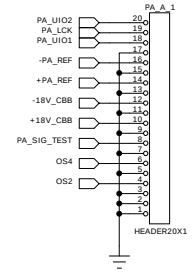


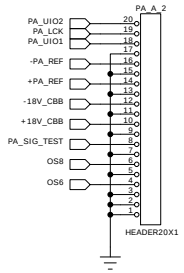


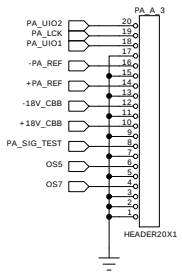


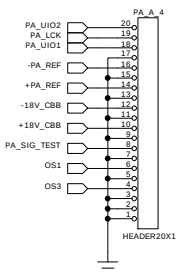












Post Amp CONNECTORS

COMPANY: THE OHIO STATE UNIVERSITY DEPARTMENT OF ASTRONOMY IMAGING SCIENCES LABORATORY					
TITLE: CBB-K-PA-CONNECTORS					
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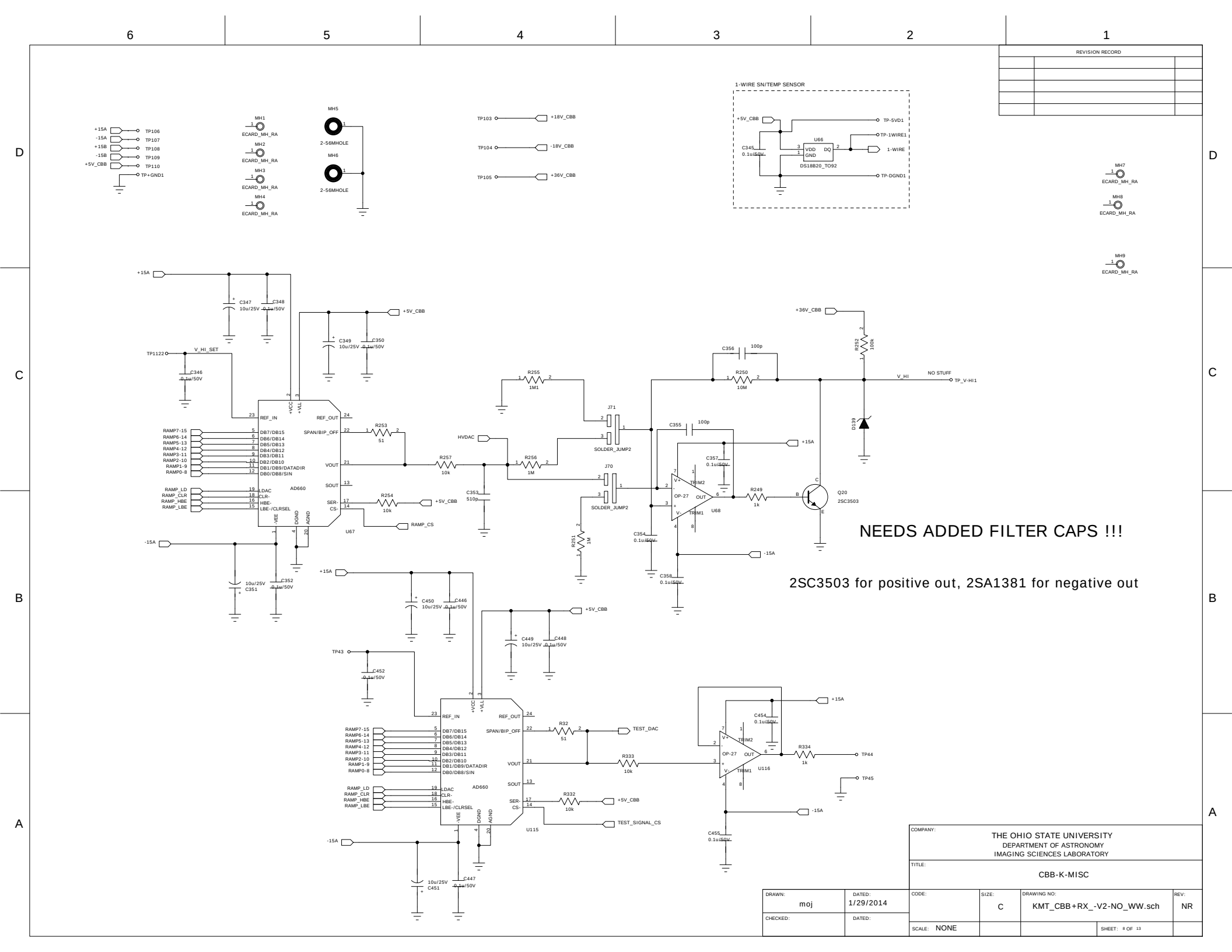
CHECKED:	DATED:	SCALE: NONE		SHEET: 7 OF 13	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+5V_CBB
TP-5VD1
TP-1WIRE1
1-WIRE
TP-DGND1
U66
VDD
DQ
GND
DS18B20_TO92
C345
0.1u/50V
MH1
MH2
MH3
MH4
MH5
MH6
MH7
MH8
MH9
ECARD_MH_RA
2-56MHOLE
TP103
TP104
TP105
+18V_CBB
-18V_CBB
+36V_CBB
+15A
-15A
+15B
-15B
+5V_CBB
TP106
TP107
TP108
TP109
TP110
TP+GND1
TP1122
V_HI_SET
C346
C347
10u/25V
C348
0.1u/50V
C349
C350
C351
C352
C353
510p
C354
C355
100p
C356
C357
C358
R249
1k
R250
10M
R251
1M
R252
100k
R253
51
R254
10k
R255
1M1
R256
1M
R257
10k
J70
J71
SOLDER_JUMP2
HVDAC
V_HI
NO STUFF
TP_V-HI1
D139
Q20
2SC3503
U67
U68
AD660
OP-27
TRIM1
TRIM2
REF_IN
REF_OUT
SPAN/BIP_OFF
VOUT
SOUT
SER-
CS-
LDAC
CLR-
HBE-
LBE-/CLRSEL
-VEE
DGND
AGND
+VCC
+VLL
RAMP7-15
RAMP6-14
RAMP5-13
RAMP4-12
RAMP3-11
RAMP2-10
RAMP1-9
RAMP0-8
DB7/DB15
DB6/DB14
DB5/DB13
DB4/DB12
DB3/DB11
DB2/DB10
DB1/DB9/DATADIR
DB0/DB8/SIN
RAMP_LD
RAMP_CLR
RAMP_HBE
RAMP_LBE
RAMP_CS
NEEDS ADDED FILTER CAPS !!!
2SC3503 for positive out, 2SA1381 for negative out
TP43
C450
C446
C449
C448
C452
C447
C451
C454
C455
R32
51
R333
10k
R332
10k
R334
1k
TEST_DAC
TEST_SIGNAL_CS
TP44
TP45
U115
U116
COMPANY:
THE OHIO STATE UNIVERSITY
DEPARTMENT OF ASTRONOMY
IMAGING SCIENCES LABORATORY
TITLE:
CBB-K-MISC
DRAWN:
moj
DATED:
1/29/2014
CHECKED:
DATED:
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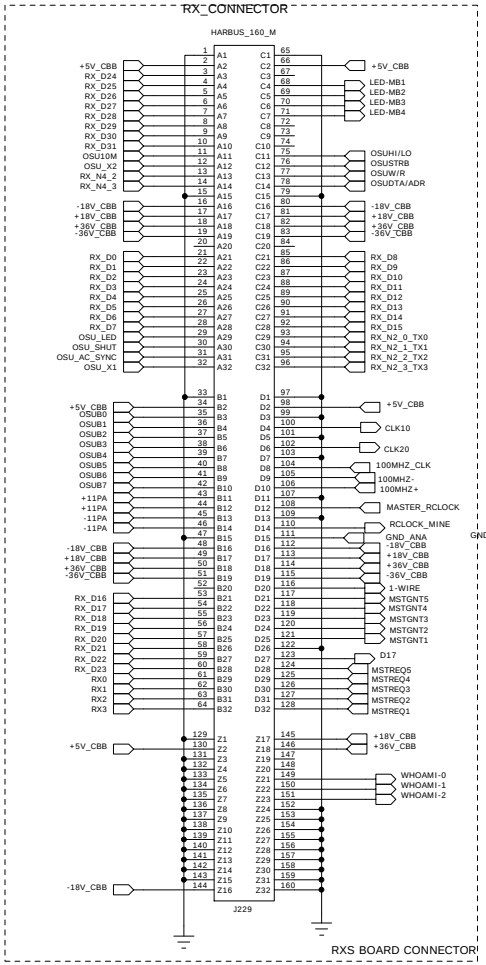
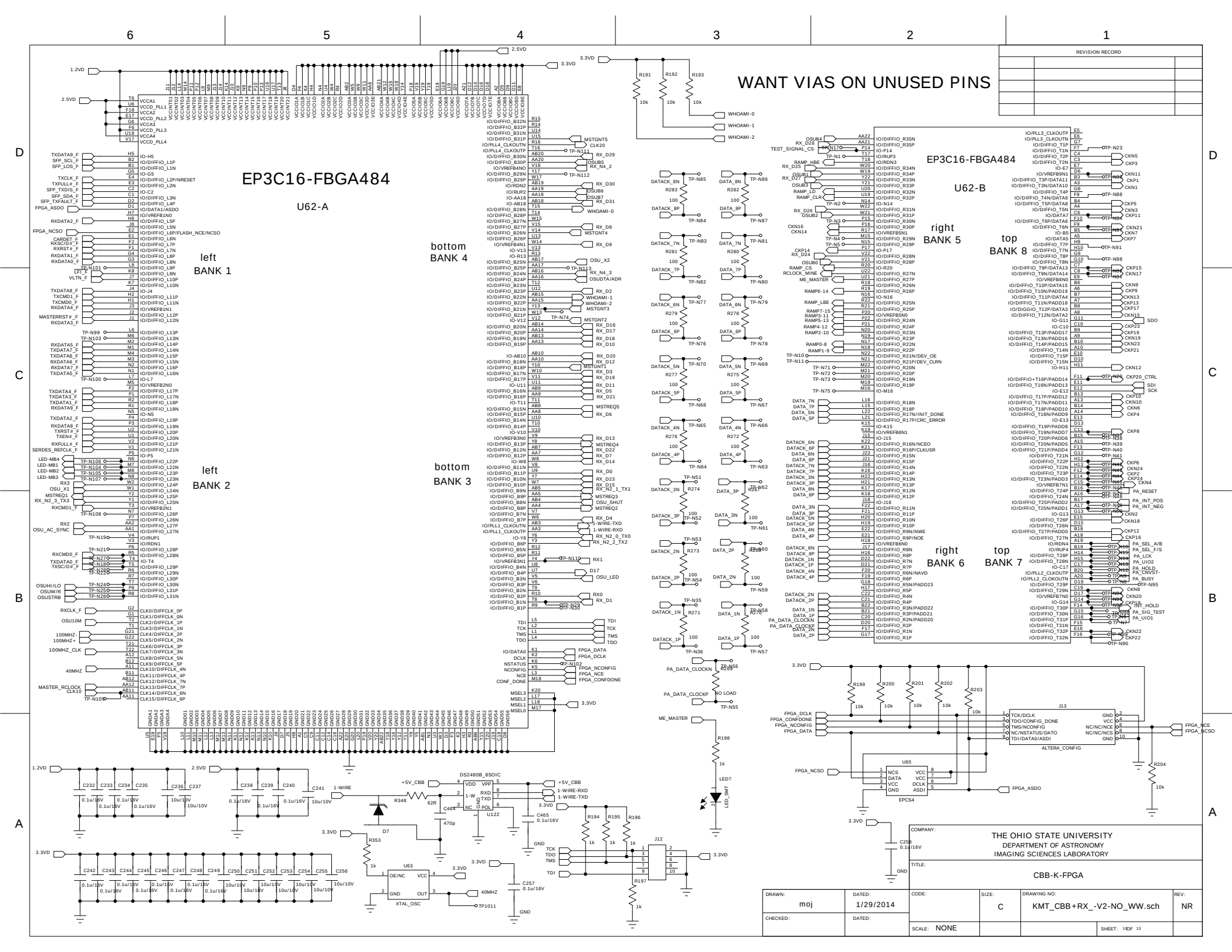
REV:
NR
SCALE:
NONE
SHEET:
8 OF 13



DO THESE AGREE WITH MODS ???

REVISION RECORD		

COMPANY: THE OHIO STATE UNIVERSITY DEPARTMENT OF ASTRONOMY IMAGING SCIENCES LABORATORY					
TITLE: CBB-K-CONNECTORS					
DRAWN: moj	DATED: 1/29/2014	CODE:	SIZE: C	DRAWING NO: KMT_CBB+RX_-V2-NO_WW.sch	REV: NR
CHECKED:	DATED:	SCALE: NONE		SHEET: 9 OF 13	


WANT VIAS ON UNUSED PINS
EP3C16-FBGA484
U62-A
left
BANK 1
EP3C16-FBGA484
U62-B
right
BANK 5
top
BANK 8
left
BANK 2
bottom
BANK 4
bottom
BANK 3
right
BANK 6
top
BANK 7
REVISION RECORD
THE OHIO STATE UNIVERSITY
DEPARTMENT OF ASTRONOMY
IMAGING SCIENCES LABORATORY
CBB-K-FPGA
DRAWN: moj
DATED: 1/29/2014
CHECKED:
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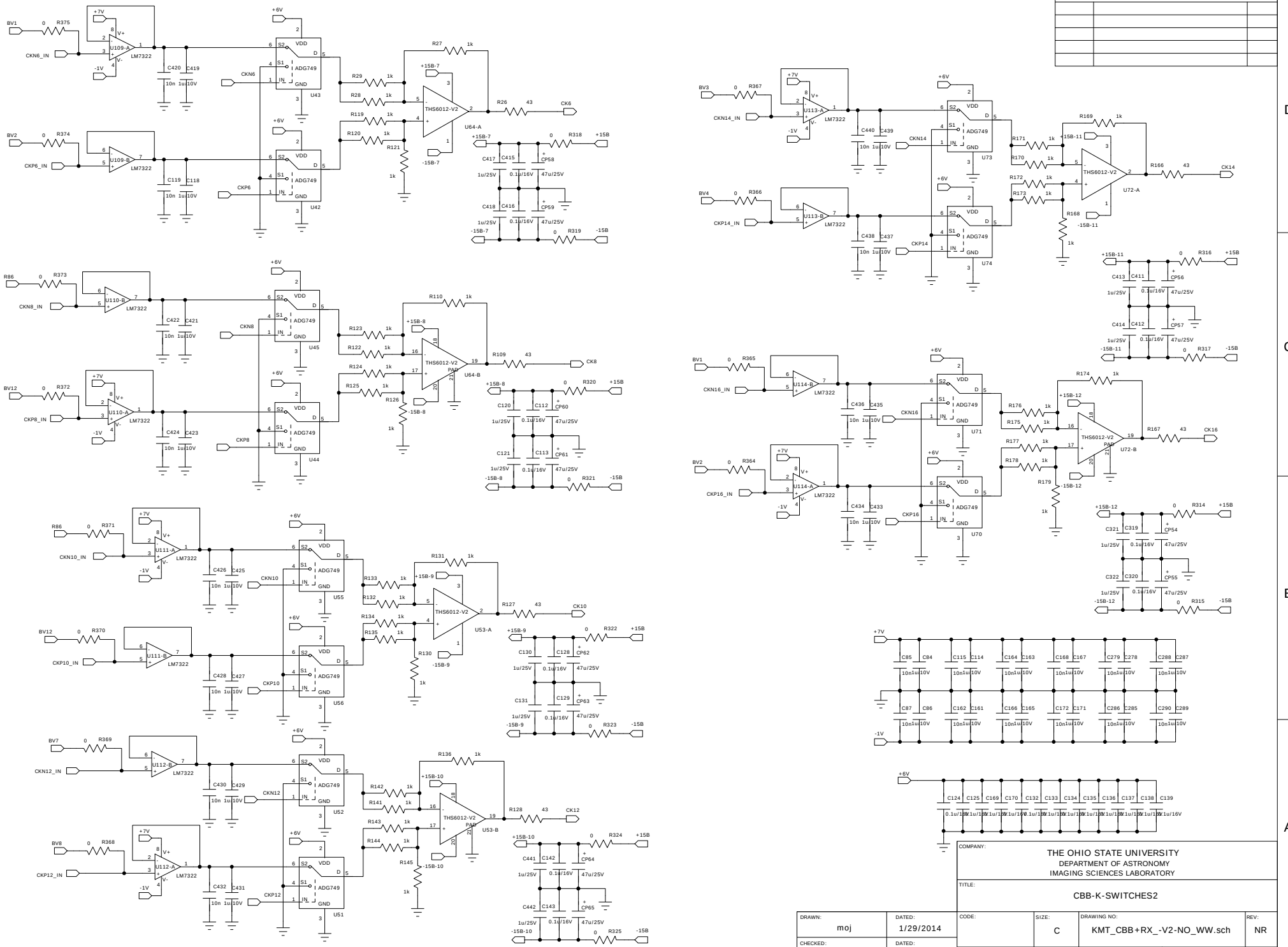
SHEET: 1 OF 13


6
5
4
3
2
1
D
C
B
A
REVISION RECORD
BV1
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CKN6_IN
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LM7322
+7V
-1V
C420
C419
10n
1u/10V
CKN6
U43
ADG749
+6V
R29
R28
R27
1k
+15B-7
THS6012-V2
U64-A
R26
43
CK6
R119
R120
R121
-15B-7
BV2
R374
CKP6_IN
U109-B
C119
C118
CKP6
U42
C417
C415
CP58
1u/25V
0.1u/16V
47u/25V
C418
C416
CP59
R318
+15B
R319
-15B
R86
R373
CKN8_IN
U110-B
C422
C421
CKN8
U45
R110
R123
R122
+15B-8
R109
CK8
R124
R125
R126
-15B-8
BV12
R372
CKP8_IN
U110-A
C424
C423
CKP8
U44
C120
C112
CP60
C121
C113
CP61
R320
R321
BV3
R367
CKN14_IN
U113-A
C440
C439
CKN14
U73
R169
R171
R170
R166
CK14
U72-A
BV4
R366
CKP14_IN
U113-B
C438
C437
CKP14
U74
R172
R173
R168
-15B-11
+15B-11
C413
C411
CP56
C414
C412
CP57
R316
R317
BV1
R365
CKN16_IN
U114-B
C436
C435
CKN16
U71
R174
R176
R175
R167
CK16
U72-B
R177
R178
R179
-15B-12
+15B-12
BV2
R364
CKP16_IN
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C434
C433
CKP16
U70
C321
C319
CP54
C322
C320
CP55
R314
R315
BV12
R370
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C427
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U56
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R133
R132
R127
CK10
R134
R135
R130
-15B-9
+15B-9
C130
C128
CP62
C131
C129
CP63
R322
R323
BV7
R369
CKN12_IN
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C429
CKN12
U52
R136
R142
R141
R128
CK12
R143
R144
R145
-15B-10
+15B-10
C441
C142
CP64
C442
C143
CP65
R324
R325
BV8
R368
CKP12_IN
U112-A
C432
C431
CKP12
U51
BV
R
CKN
CKP
U
C
CP
+7V
-1V
+6V
+15B
-15B
+15B-7
-15B-7
+15B-8
-15B-8
+15B-9
-15B-9
+15B-10
-15B-10
+15B-11
-15B-11
+15B-12
-15B-12
C85
C84
C115
C114
C164
C163
C168
C167
C279
C278
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C86
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C166
C165
C172
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C286
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C290
C289
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C125
C169
C170
C132
C133
C134
C135
C136
C137
C138
C139
COMPANY:
THE OHIO STATE UNIVERSITY
DEPARTMENT OF ASTRONOMY
IMAGING SCIENCES LABORATORY
TITLE:
CBB-K-SWITCHES2
DRAWN:
moj
DATED:
1/29/2014
CHECKED:
DATED:
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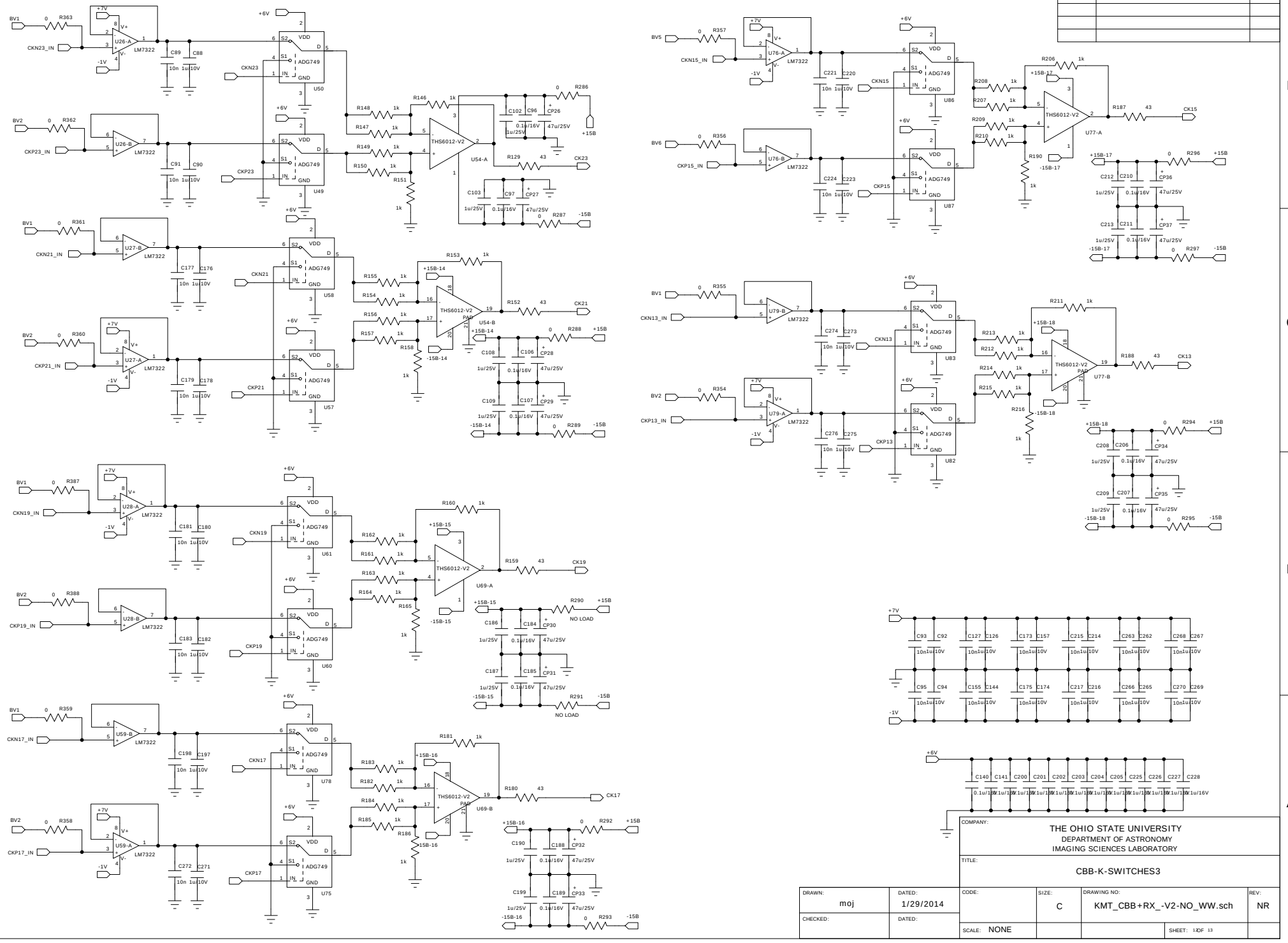
OF
13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4
3
2
1
D
C
B
A
REVISION RECORD
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LM7322
+7V
-1V
C89
C88
10n
1u/10V
+6V
VDD
S2
D
S1
IN
GND
ADG749
U50
CKN23
R148
R147
R149
R150
R151
R146
1k
THS6012-V2
U54-A
C102
C96
CP26
0.1u/16V
1u/25V
47u/25V
R286
+15B
R129
43
CK23
C103
C97
CP27
R287
-15B
BV2
R362
CKP23_IN
U26-B
C91
C90
CKP23
U49
BV1
R361
CKN21_IN
U27-B
C177
C176
CKN21
U58
R153
R155
R154
R156
R157
R158
+15B-14
-15B-14
U54-B
THS6012-V2
PAP
R152
CK21
C108
C106
CP28
R288
C109
C107
CP29
R289
BV2
R360
CKP21_IN
U27-A
C179
C178
CKP21
U57
BV1
R387
CKN19_IN
U28-A
C181
C180
CKN19
U61
R160
R162
R161
R163
R164
R165
+15B-15
-15B-15
U69-A
R159
CK19
C186
C184
CP30
R290
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C187
C185
CP31
R291
BV2
R388
CKP19_IN
U28-B
C183
C182
CKP19
U60
BV1
R359
CKN17_IN
U59-B
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C197
CKN17
U78
R181
R183
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R184
R185
R186
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-15B-16
U69-B
R180
CK17
C190
C188
CP32
R292
C199
C189
CP33
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BV2
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C271
CKP17
U75
BV5
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U76-A
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C220
CKN15
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R207
R209
R210
R206
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-15B-17
U77-A
R187
CK15
R190
C212
C210
CP36
C213
C211
CP37
R296
R297
BV6
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C223
CKP15
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R355
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C273
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C203
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COMPANY:
THE OHIO STATE UNIVERSITY
DEPARTMENT OF ASTRONOMY
IMAGING SCIENCES LABORATORY
TITLE:
CBB-K-SWITCHES3
DRAWN:
moj
DATED:
1/29/2014
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SCALE:
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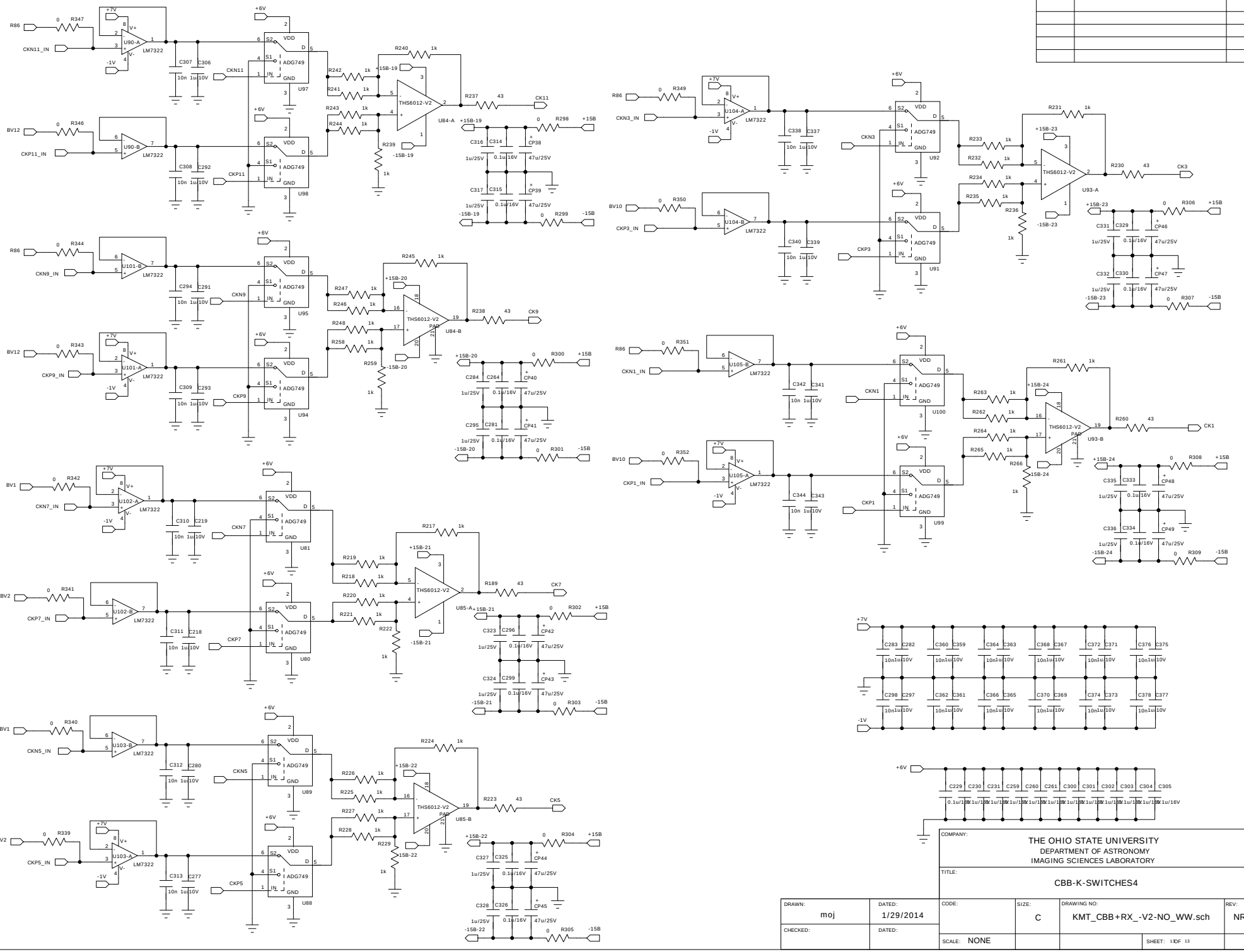
12
OF
13


6
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A
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U90-A
U90-B
U101-B
U101-A
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THS6012-V2
U97
U98
U95
U94
U81
U80
U89
U88
U92
U91
U100
U99
U84-A
U84-B
U85-A
U85-B
U93-A
U93-B
CKN11_IN
CKP11_IN
CKN9_IN
CKP9_IN
CKN7_IN
CKP7_IN
CKN5_IN
CKP5_IN
CKN3_IN
CKP3_IN
CKN1_IN
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+15B-22
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+15B-23
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+15B-24
-15B-24
COMPANY:
THE OHIO STATE UNIVERSITY
DEPARTMENT OF ASTRONOMY
IMAGING SCIENCES LABORATORY
TITLE:
CBB-K-SWITCHES4
DRAWN:
moj
DATED:
1/29/2014
CHECKED:
DATED:
CODE:
SIZE:
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DRAWING NO:
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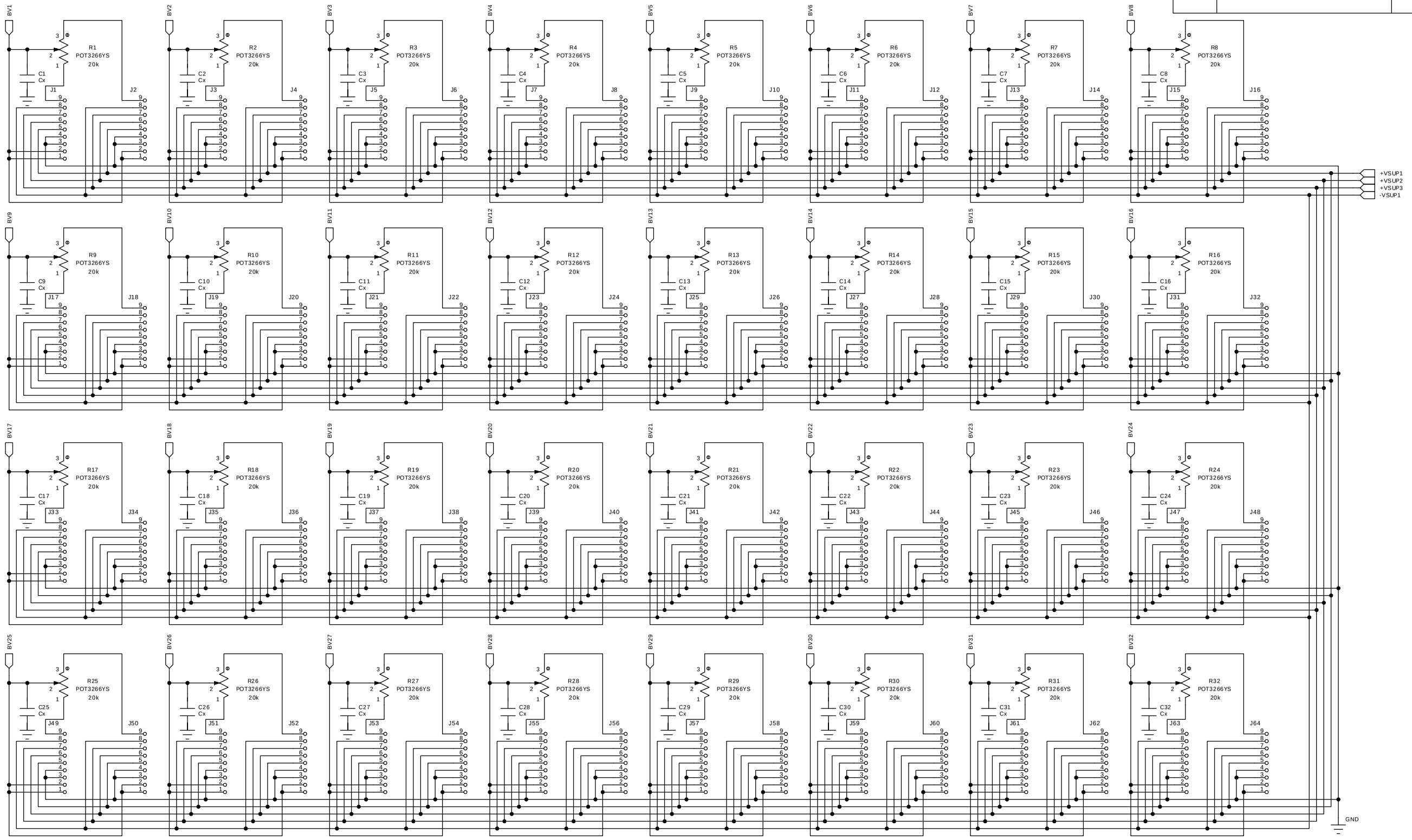
REV:
NR
SCALE:
NONE
SHEET:
1 OF 13

REVISION RECORD		



DRAWN: PAC	DATED: 21MAY2006		
CHECKED:	DATED:		

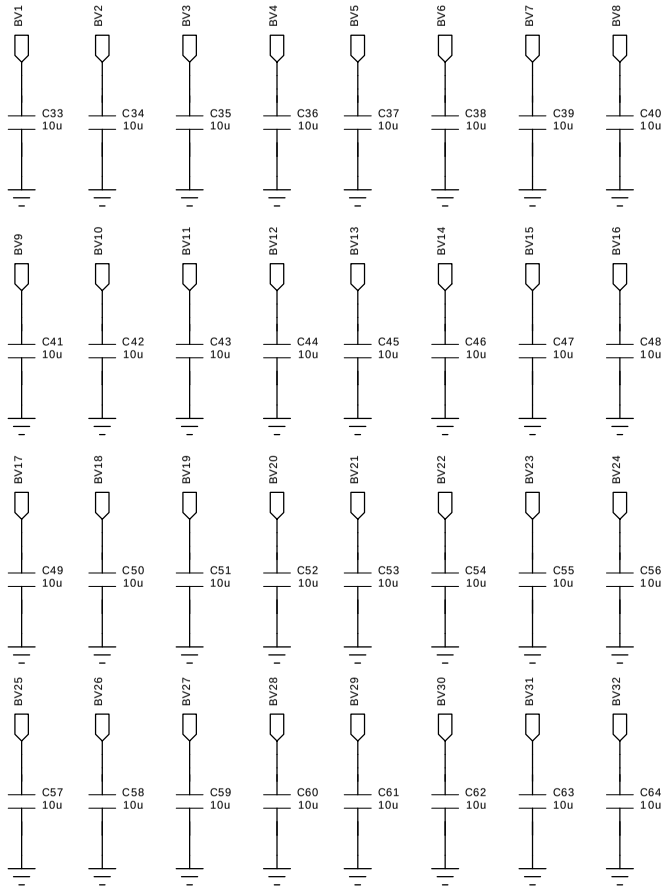
COMPANY: THE OHIO STATE UNIVERSITY
DEPARTMENT OF ASTRONOMY
IMAGING SCIENCE LABORATORY

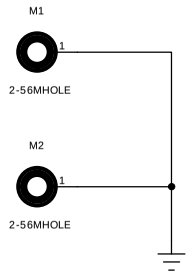
TITLE: POT MODULE

CODE:	SIZE:	DRAWING NO:	REV:
	C	POTMOD.SCH	NR

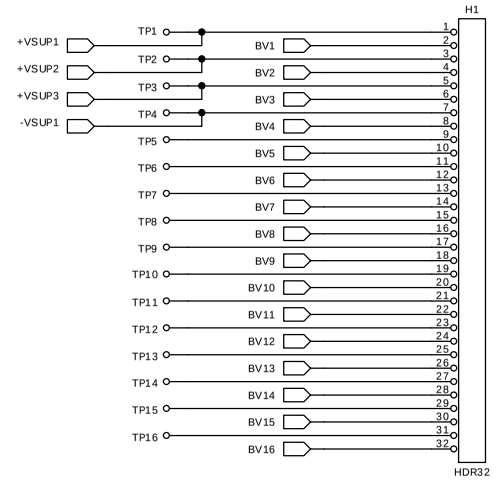
SCALE: NONE SHEET: 1 OF 2

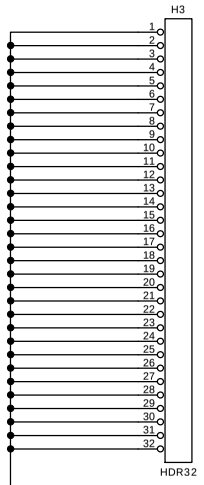
REVISION RECORD		

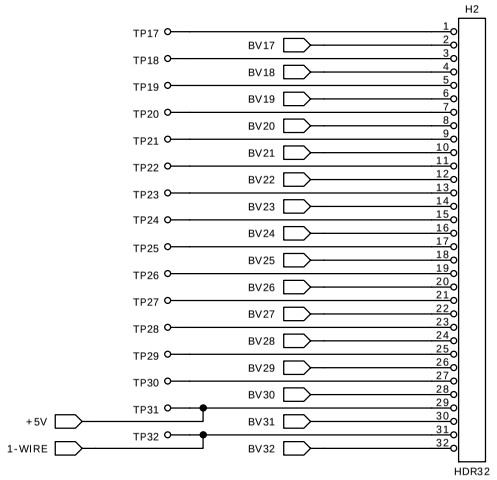


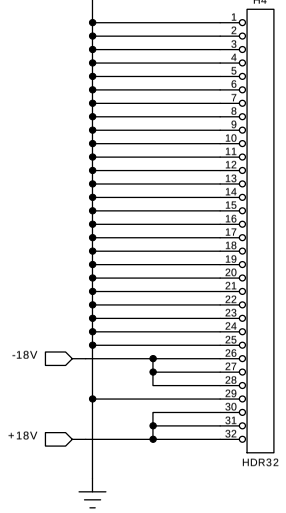


1-WIRE S/N TEMPERATURE SENSOR









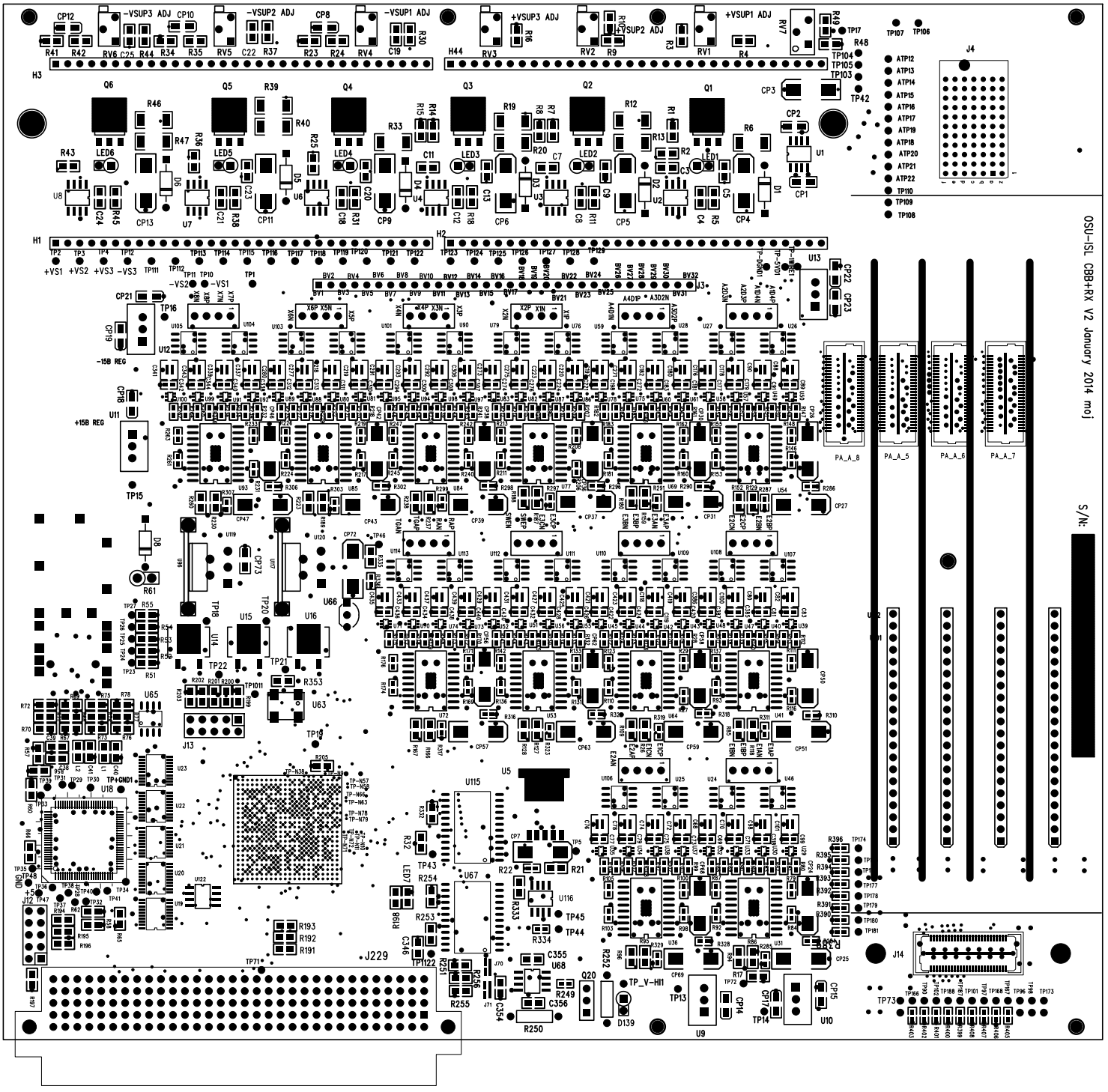
COMPANY:	THE OHIO STATE UNIVERSITY DEPARTMENT OF ASTRONOMY IMAGING SCIENCE LABORATORY
TITLE:	POT MODULE

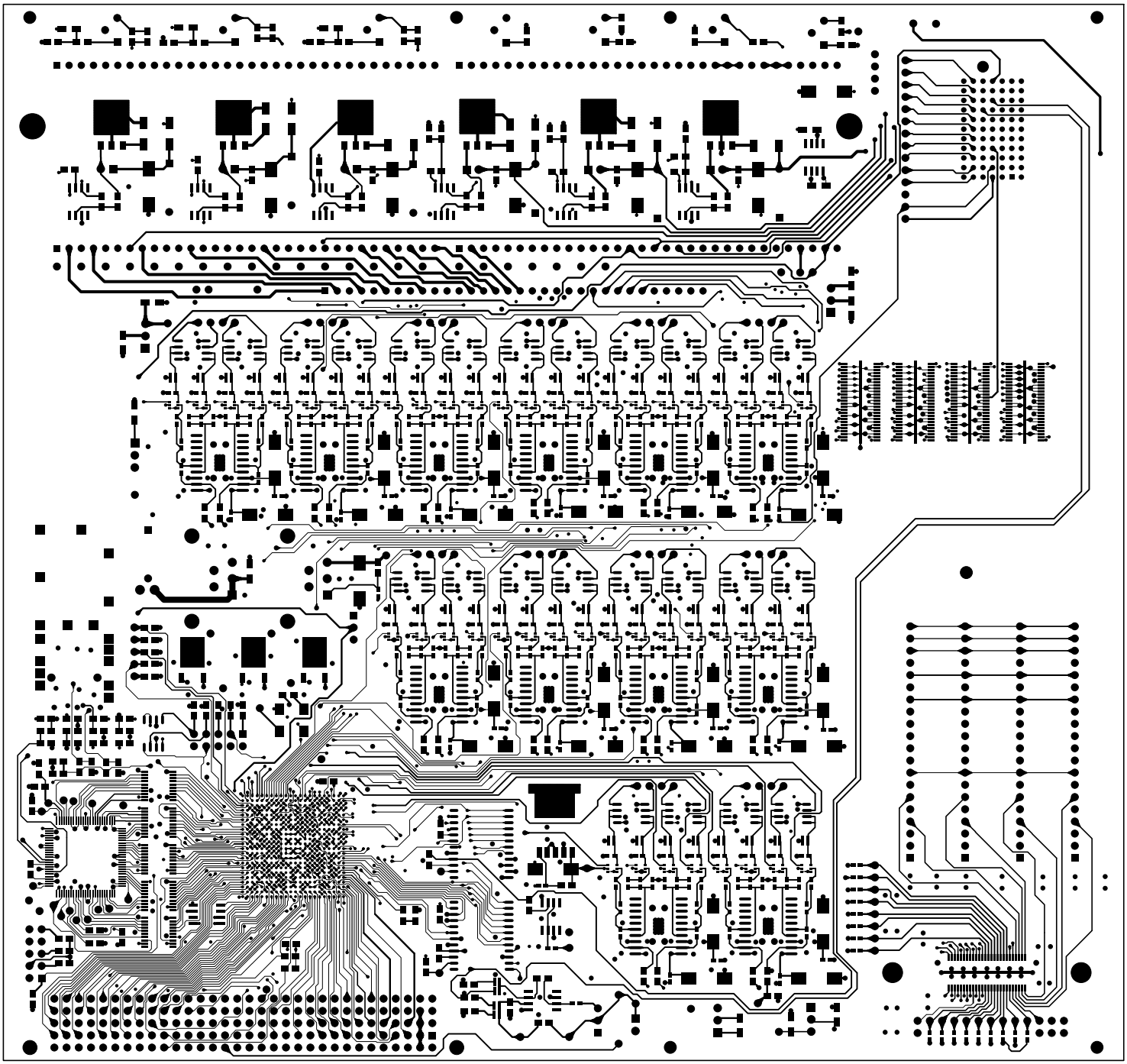
CODE:	SIZE:	DRAWING NO:	REV:
	C	POTMOD.SCH	NR

DRAWN:	DATED:
PAC	21MAY2006
CHECKED:	DATED:

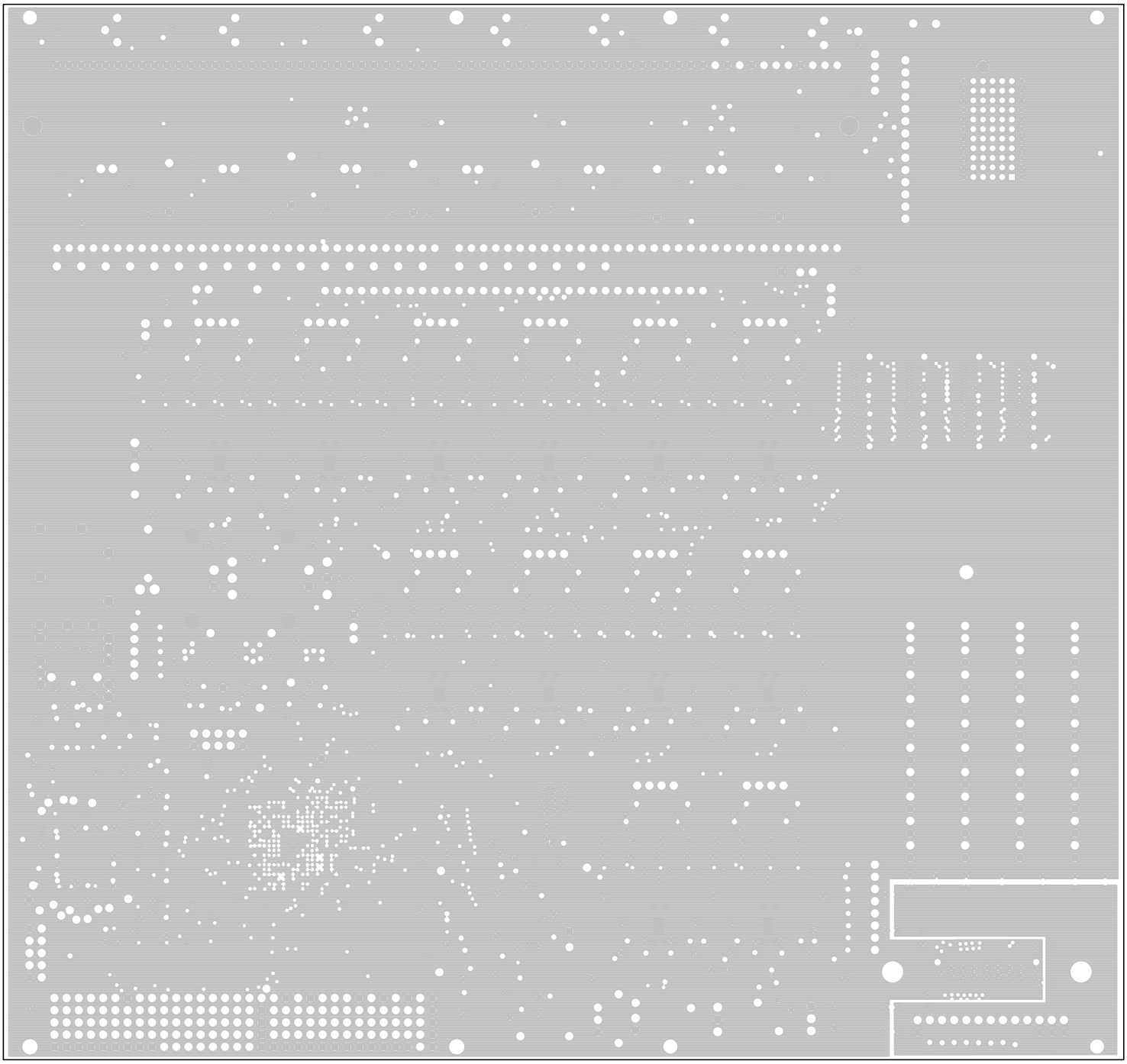
SCALE: NONE

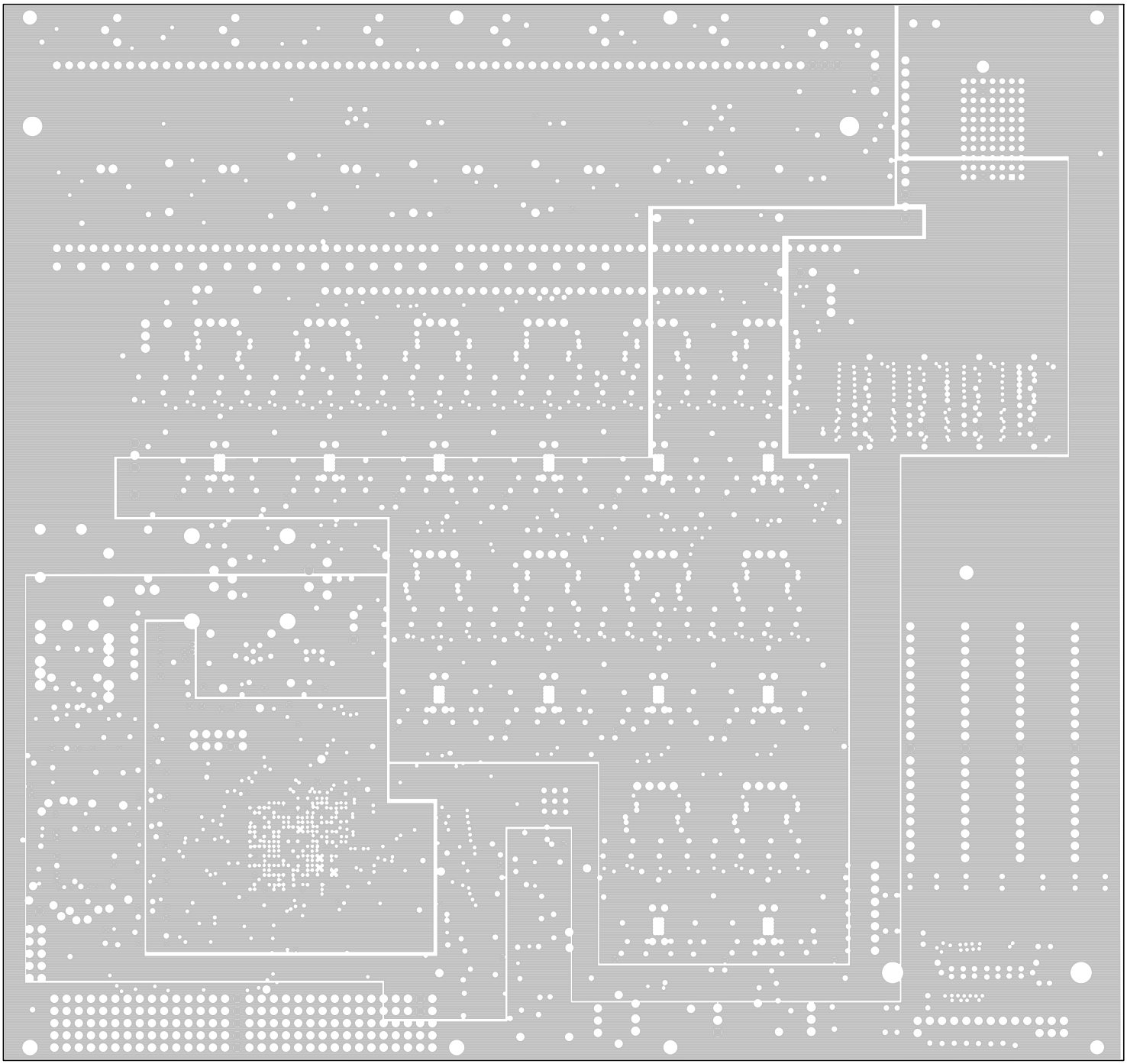
SHEET: 2 OF 2

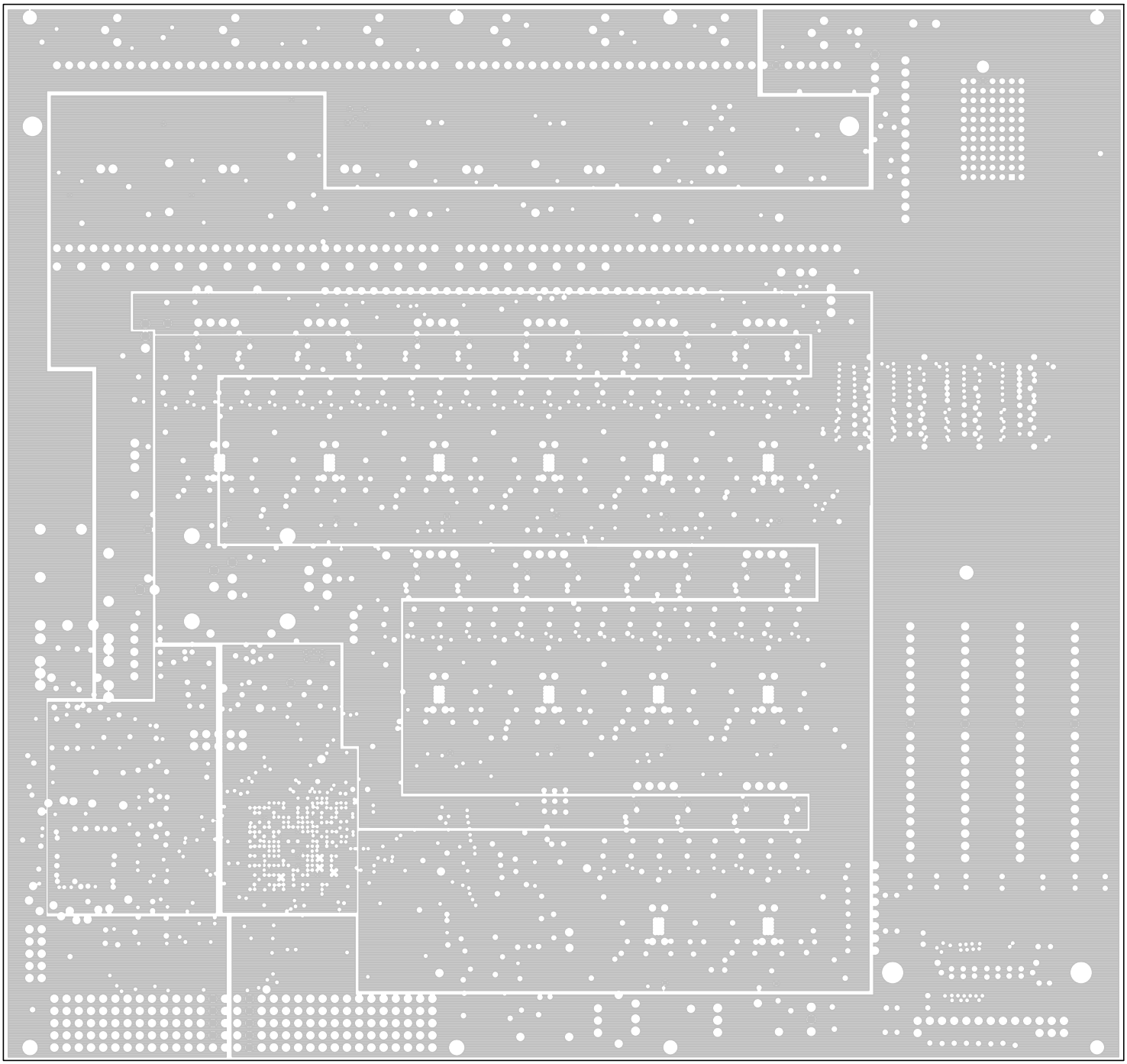

-VSUP3 ADJ
-VSUP2 ADJ
-VSUP1 ADJ
+VSUP3 ADJ
+VSUP2 ADJ
+VSUP1 ADJ
OSU-ISL CBB+RX V2 January 2014 moj
S/N:
-15B REG
+15B REG
PA_A_8
PA_A_5
PA_A_6
PA_A_7
J229

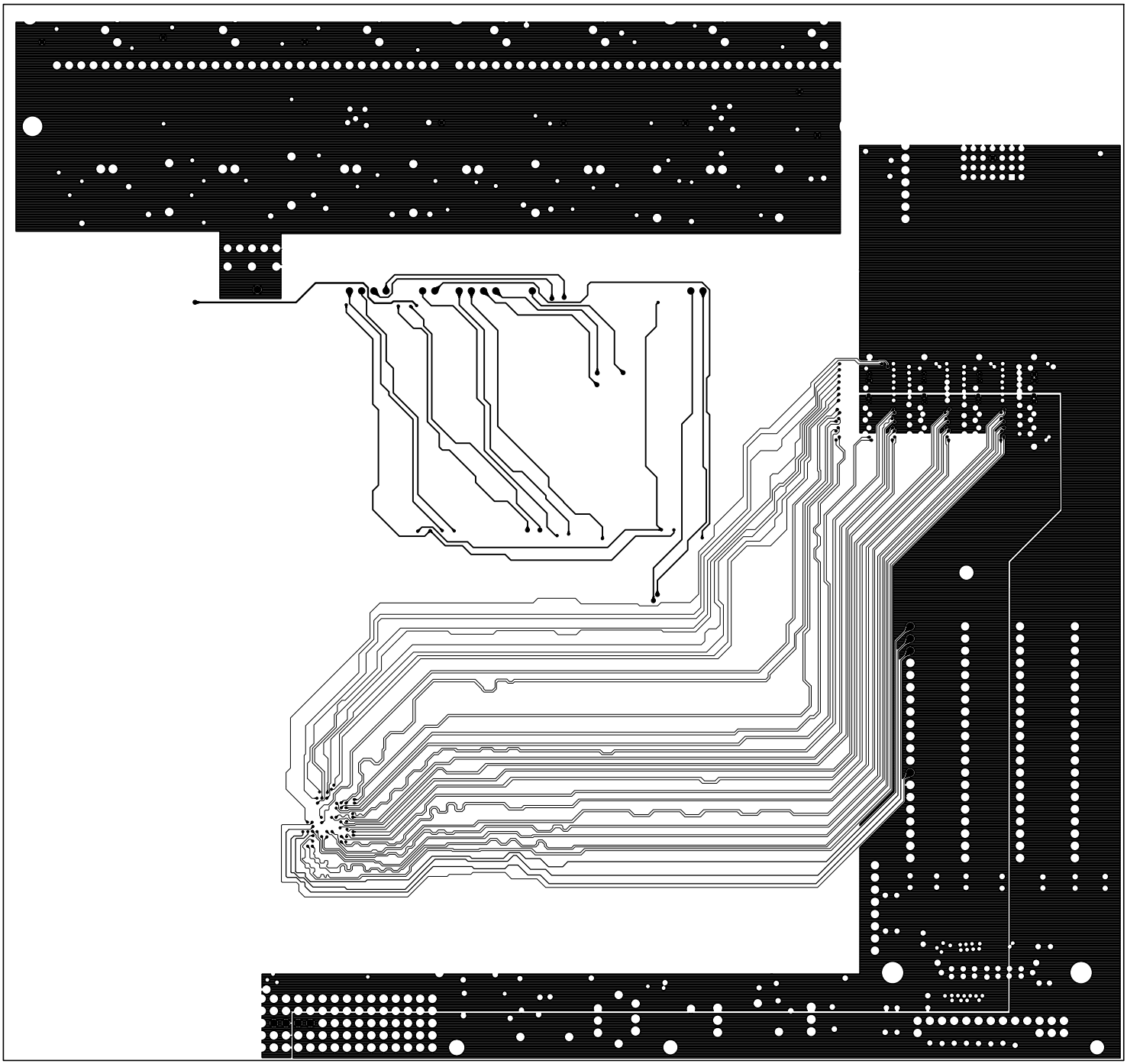


KMT_CBB+RX-V2-NO_WW.pcb - Mon Jun 23 15:25:58 2014

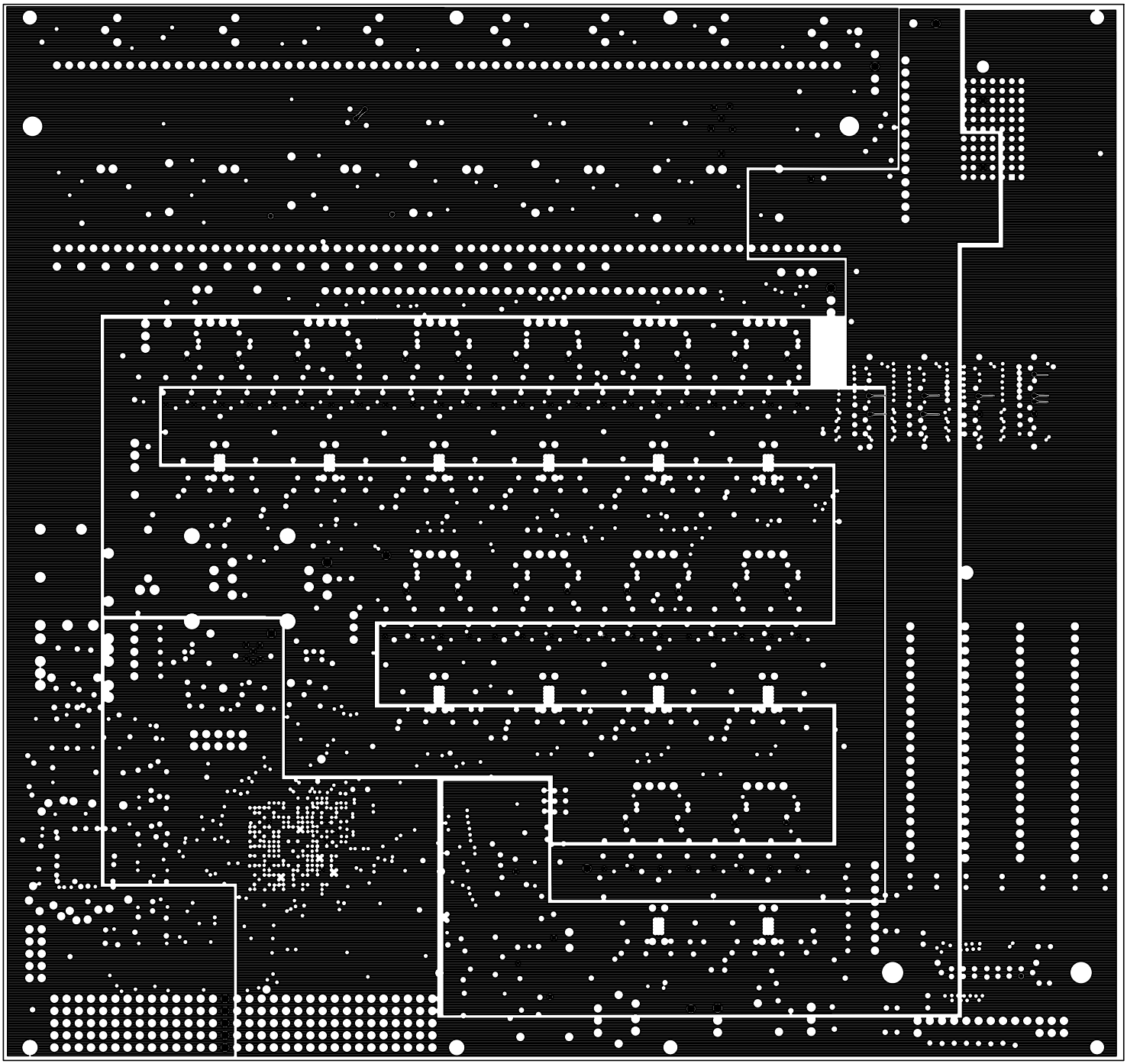


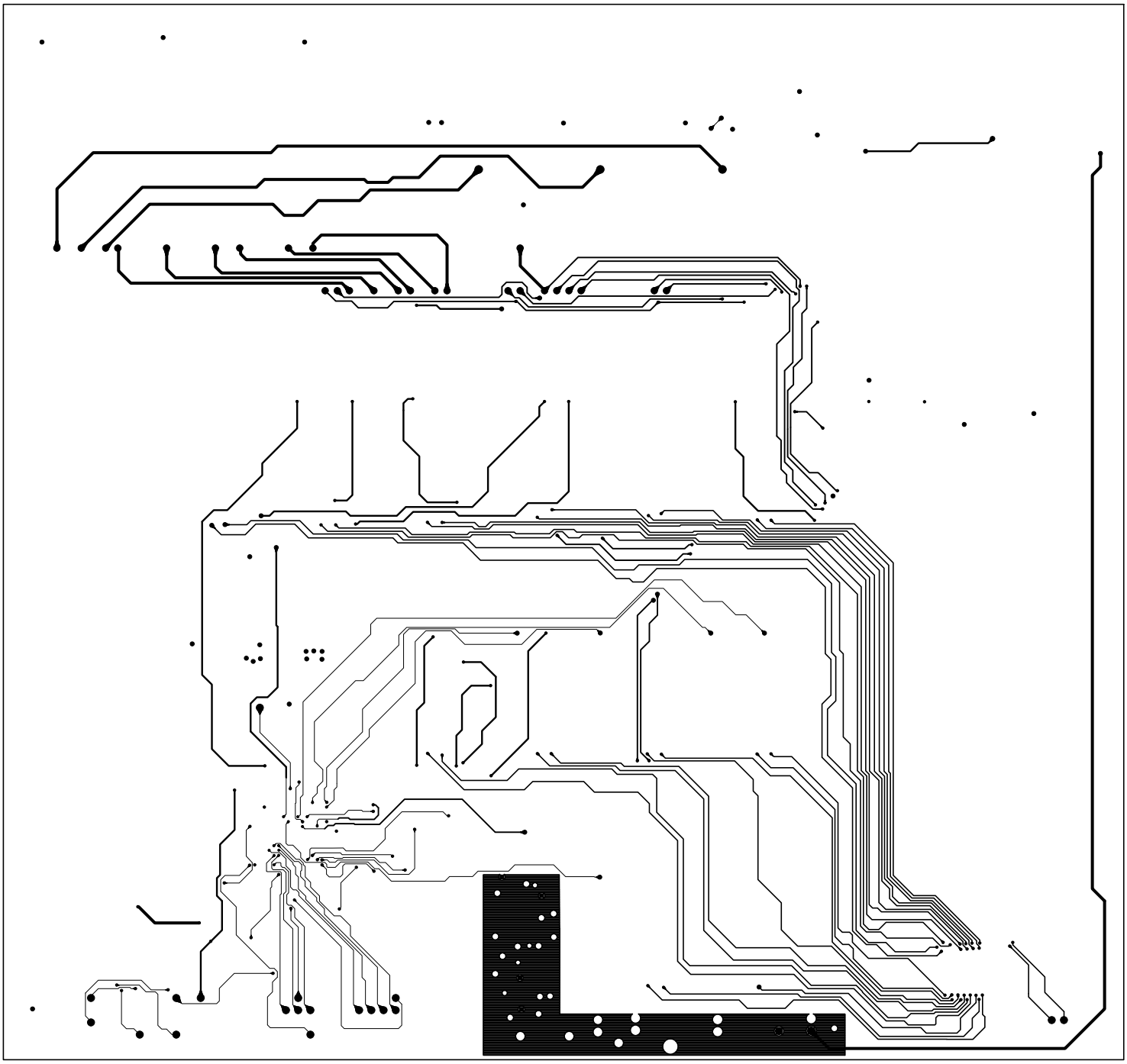




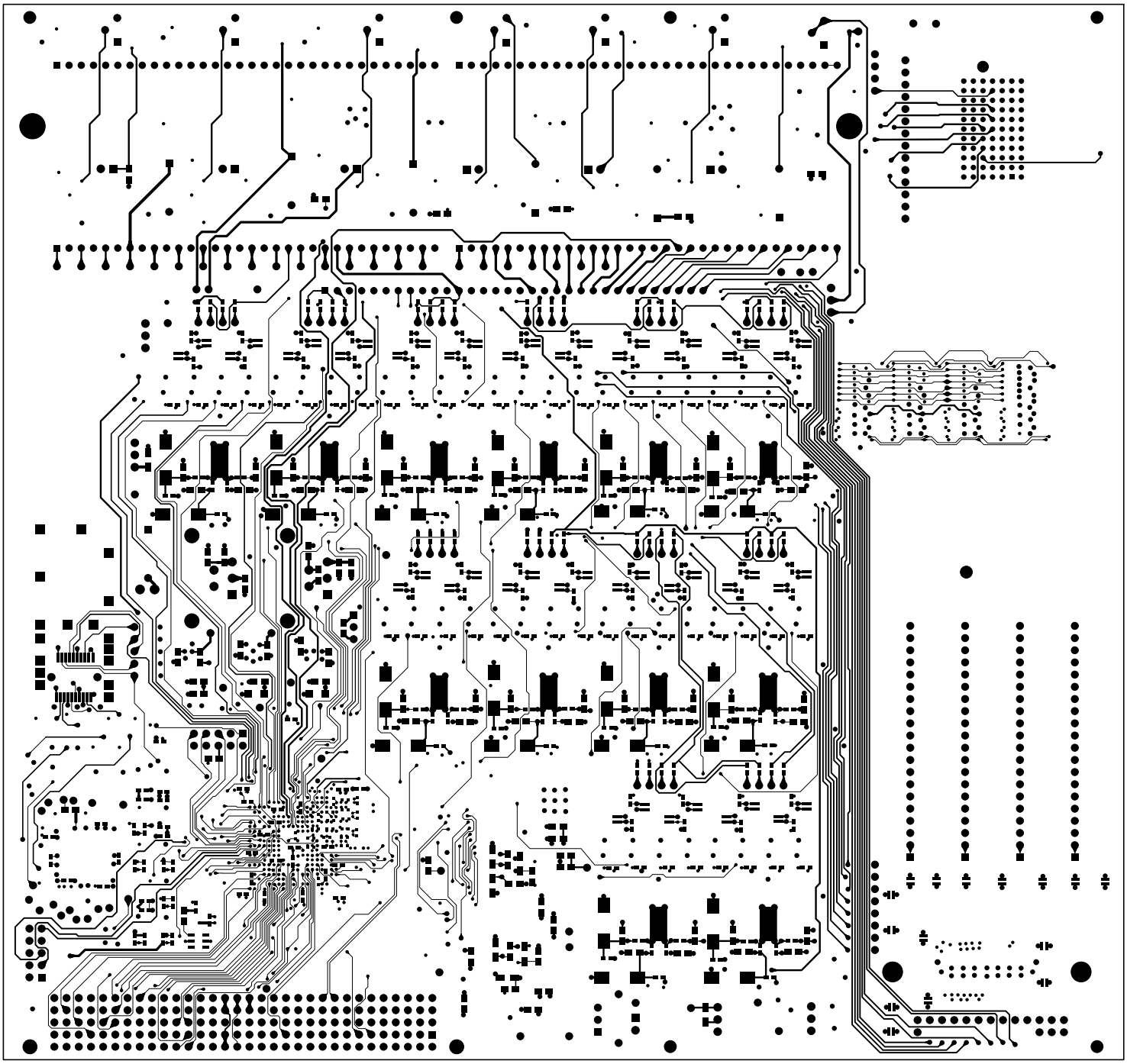


KMT_CBB+RX-V2-NO_WW.pcb - Mon Jun 23 15:26:39 2014

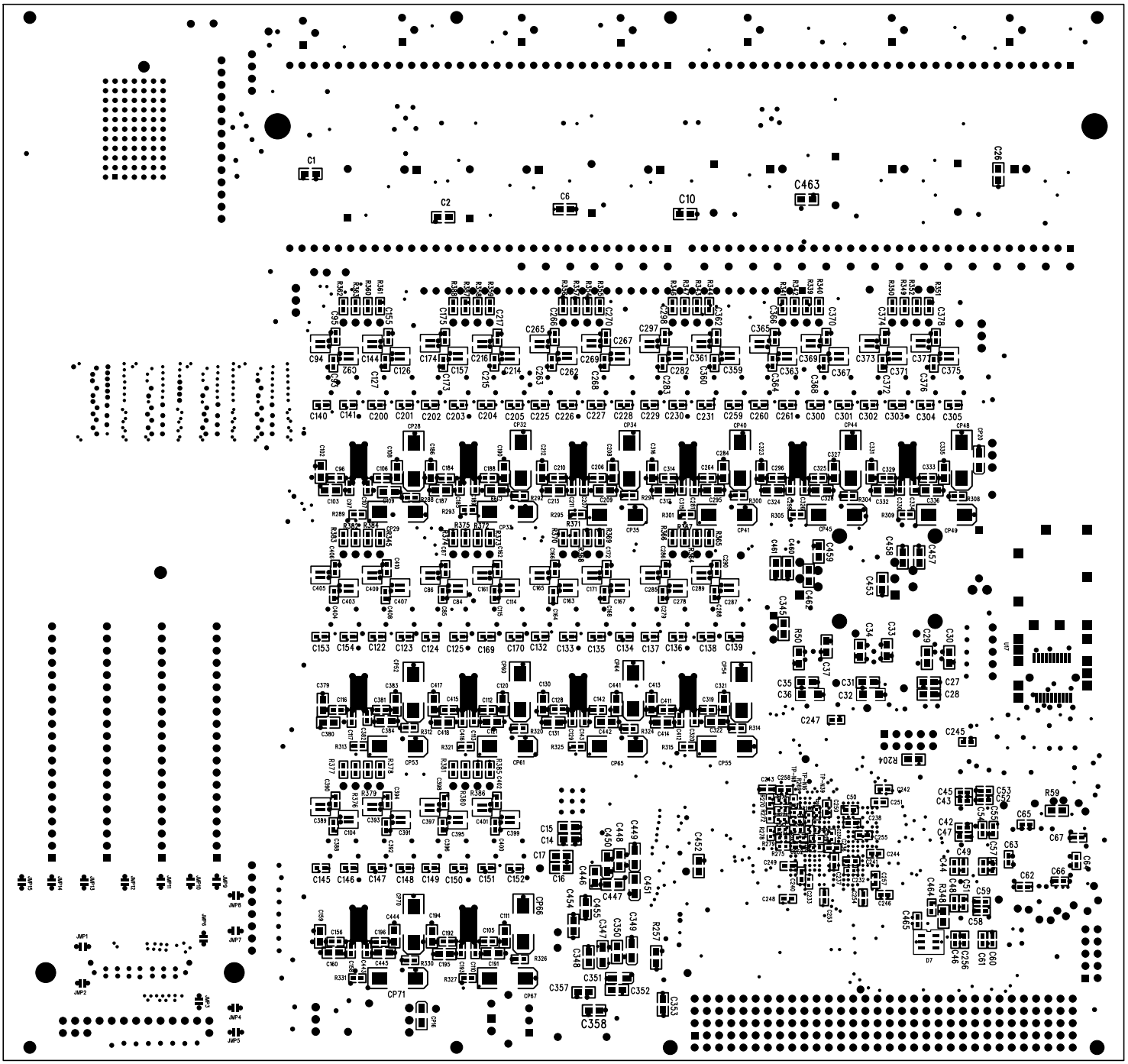




KMT_CBB+RX-V2-NO_WW.pcb - Mon Jun 23 15:27:23 2014

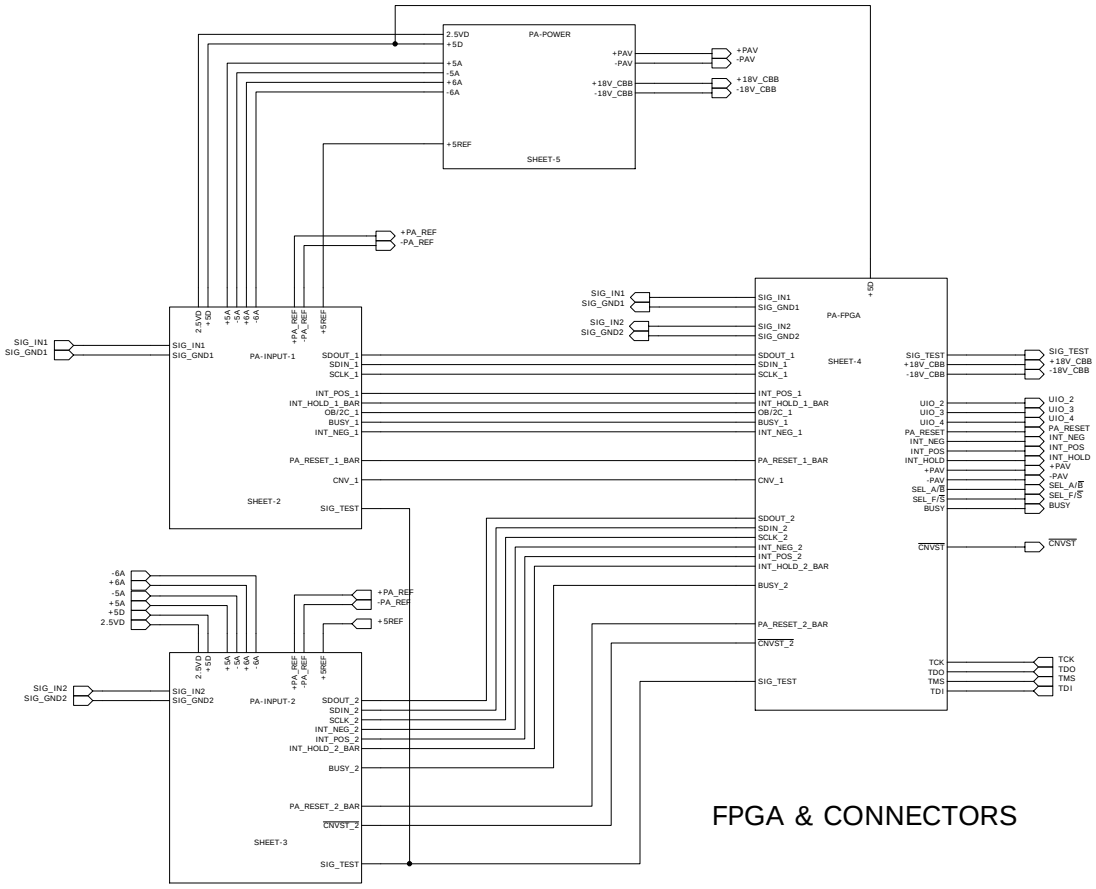


KMT_CBB+RX-V2-NO_WW.pcb - Mon Jun 23 15:27:42 2014



REVISION RECORD		

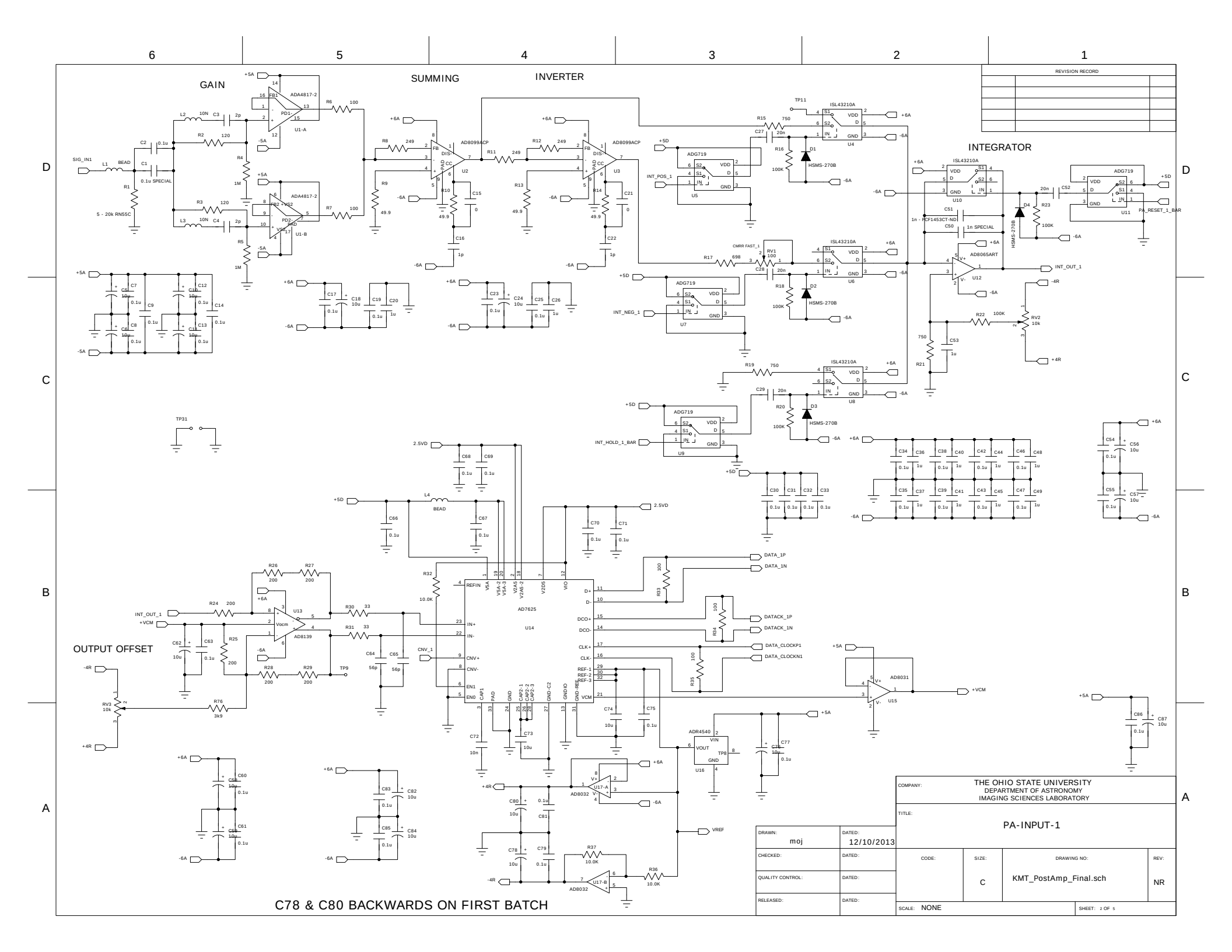
POWER SUPPLIES

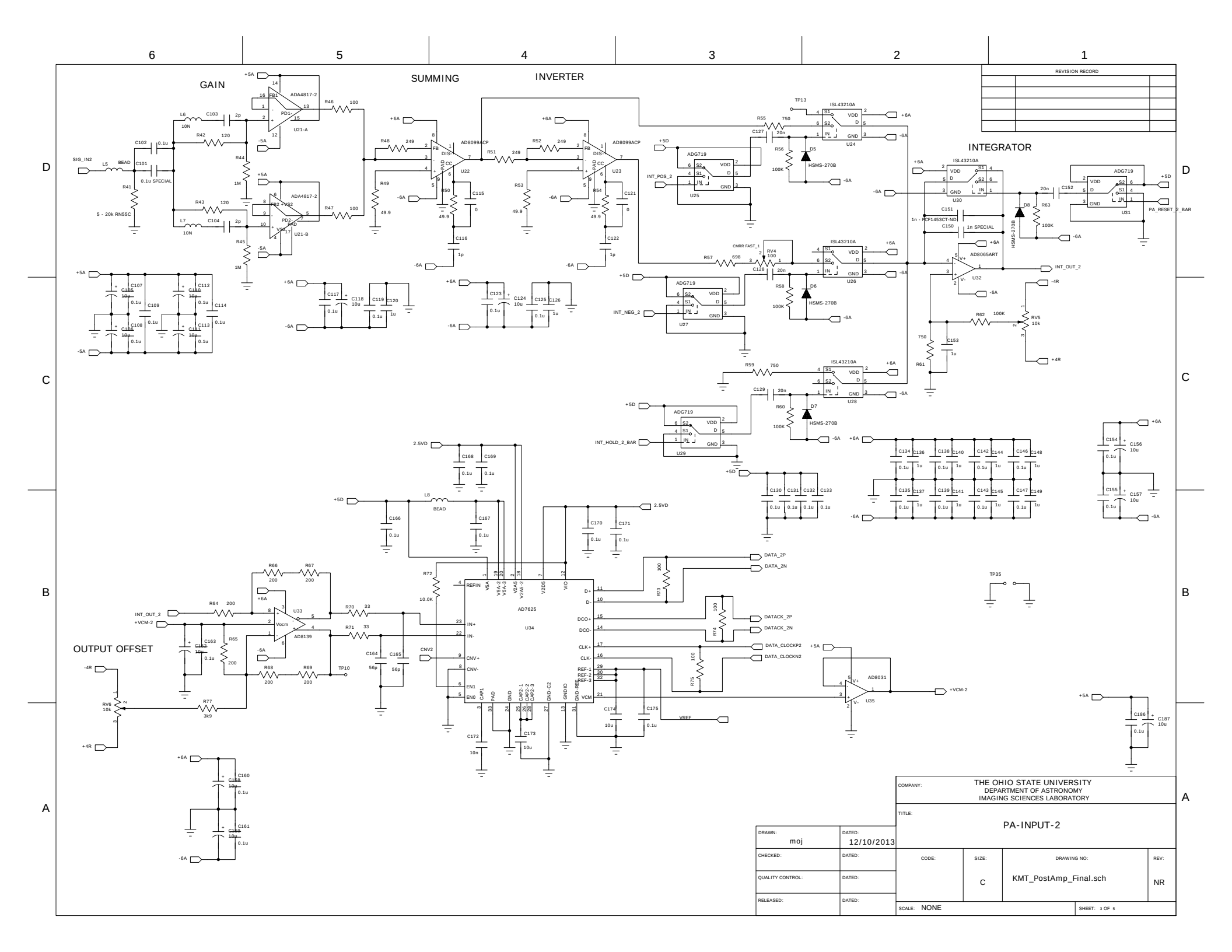


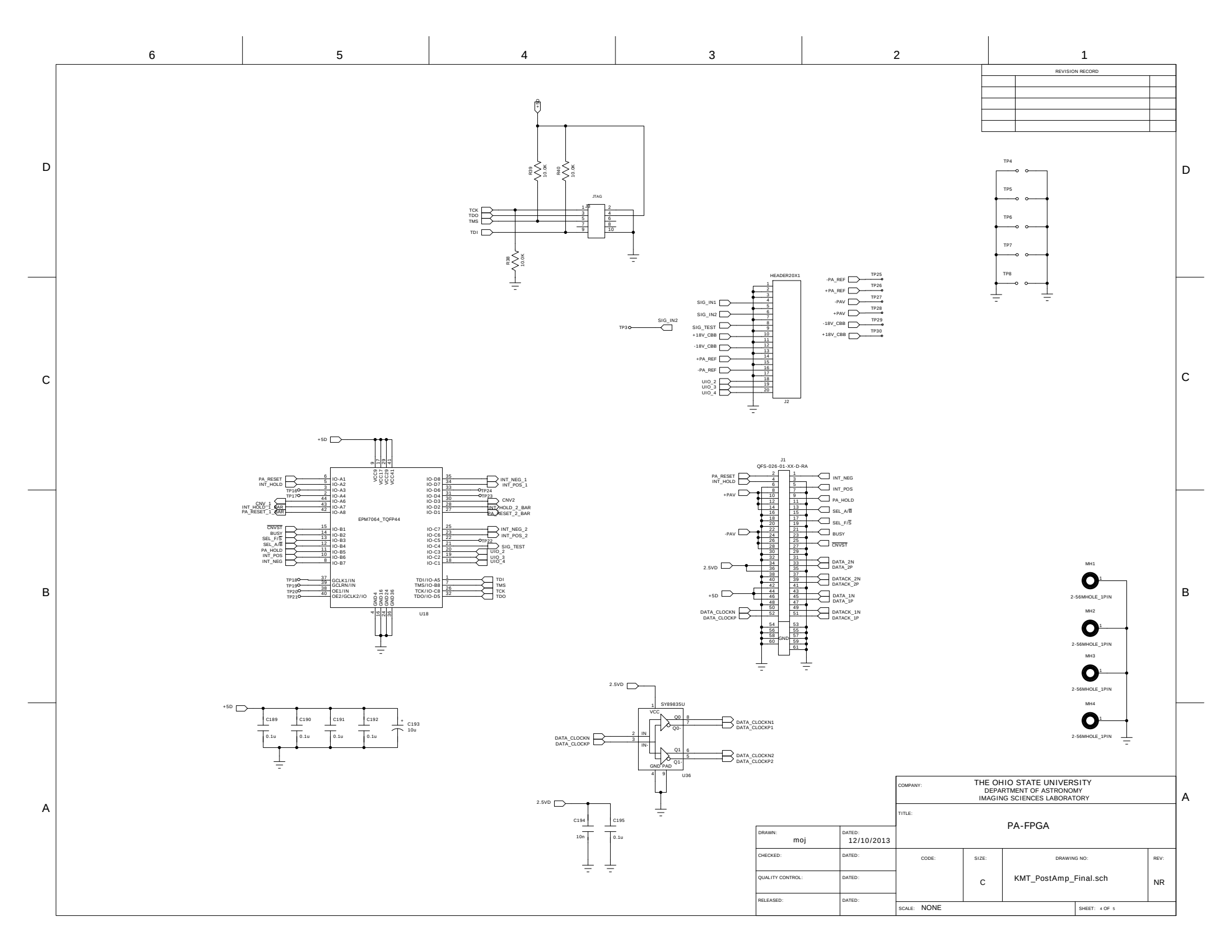
FPGA & CONNECTORS

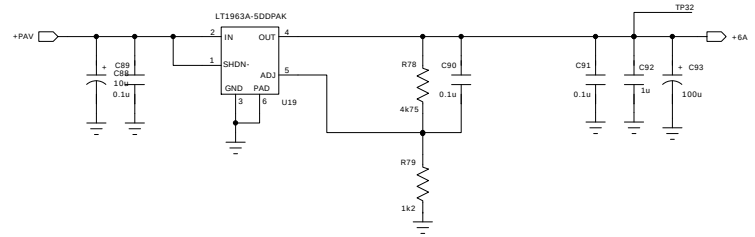
INPUTS & DIGITIZING

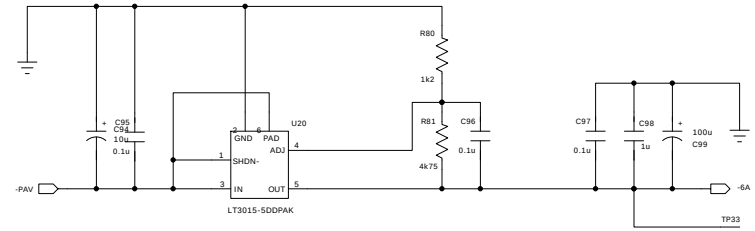
DRAWN: moj	DATED: 12/10/2013	COMPANY: THE OHIO STATE UNIVERSITY DEPARTMENT OF ASTRONOMY IMAGING SCIENCES LABORATORY	
CHECKED:	DATED:	TITLE: KTM_POSTAMP	
QUALITY CONTROL:	DATED:	CODE:	SIZE: C
RELEASED:	DATED:	DRAWING NO: KMT_PostAmp_Final.sch	REV: NR
		SCALE: NONE	SHEET: 1 OF 5

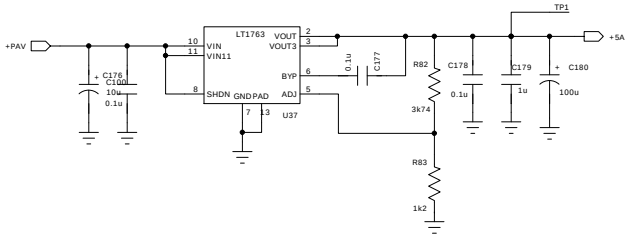

GAIN
SUMMING
INVERTER
INTEGRATOR
OUTPUT OFFSET
REVISION RECORD
C78 & C80 BACKWARDS ON FIRST BATCH
COMPANY: THE OHIO STATE UNIVERSITY
DEPARTMENT OF ASTRONOMY
IMAGING SCIENCES LABORATORY
TITLE: PA-INPUT-1
DRAWN: moj
DATED: 12/10/2013
CHECKED:
QUALITY CONTROL:
RELEASED:
CODE:
SIZE: C
DRAWING NO: KMT_PostAmp_Final.sch
REV: NR
SCALE: NONE
SHEET: 2 OF 5

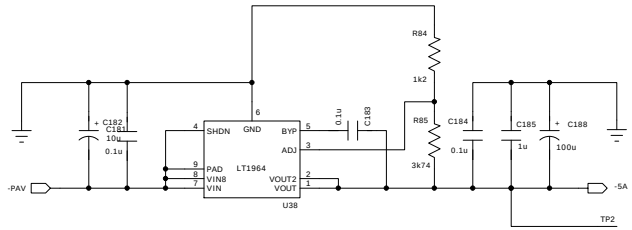

GAIN
SUMMING
INVERTER
INTEGRATOR
OUTPUT OFFSET
REVISION RECORD
ADA4817-2
AD8099ACP
ISL43210A
ADG719
HSMS-270B
AD8065ART
AD7625
AD8139
AD8031
SIG_IN2
INT_POS_2
INT_NEG_2
INT_HOLD_2_BAR
INT_OUT_2
PA_RESET_2_BAR
DATA_2P
DATA_2N
DATACK_2P
DATACK_2N
DATA_CLOCKP2
DATA_CLOCKN2
VREF
+VCM-2
2.5VD
THE OHIO STATE UNIVERSITY
DEPARTMENT OF ASTRONOMY
IMAGING SCIENCES LABORATORY
PA-INPUT-2
KMT_PostAmp_Final.sch
moj
12/10/2013
NONE
SHEET: 3 OF 5


REVISION RECORD
JTAG
R39 10.0K
R40 10.0K
R38 10.0K
TCK
TDO
TMS
TDI
TP4
TP5
TP6
TP7
TP8
HEADER20X1
J2
SIG_IN1
SIG_IN2
SIG_TEST
+18V_CBB
-18V_CBB
+PA_REF
-PA_REF
UIO_2
UIO_3
UIO_4
TP3
TP25
TP26
TP27
TP28
TP29
TP30
-PA_REF
+PA_REF
-PAV
+PAV
-18V_CBB
+18V_CBB
+5D
EPM7064_TQFP44
U18
PA_RESET
INT_HOLD
CNV
INT_HOLD_1_BAR
PA_RESET_1_BAR
CNVST
BUSY
SEL_F/S
SEL_A/B
PA_HOLD
INT_POS
INT_NEG
INT_NEG_1
INT_POS_1
CNV2
INT_HOLD_2_BAR
PA_RESET_2_BAR
INT_NEG_2
INT_POS_2
SIG_TEST
TDI
TMS
TCK
TDO
J1
QFS-026-01-XX-D-RA
DATA_2N
DATA_2P
DATACK_2N
DATACK_2P
DATA_1N
DATA_1P
DATACK_1N
DATACK_1P
DATA_CLOCKN
DATA_CLOCKP
2.5VD
GND
MH1
MH2
MH3
MH4
2-56MHOLE_1PIN
C189 0.1u
C190 0.1u
C191 0.1u
C192 0.1u
C193 10u
SY89835U
VCC
IN
IN-
Q0
Q0-
Q1
Q1-
GND PAD
U36
DATA_CLOCKN1
DATA_CLOCKP1
DATA_CLOCKN2
DATA_CLOCKP2
C194 10n
C195 0.1u
COMPANY: THE OHIO STATE UNIVERSITY
DEPARTMENT OF ASTRONOMY
IMAGING SCIENCES LABORATORY
TITLE: PA-FPGA
DRAWN: moj
DATED: 12/10/2013
CHECKED:
QUALITY CONTROL:
RELEASED:
CODE:
SIZE: C
DRAWING NO: KMT_PostAmp_Final.sch
REV: NR
SCALE: NONE
SHEET: 4 OF 5





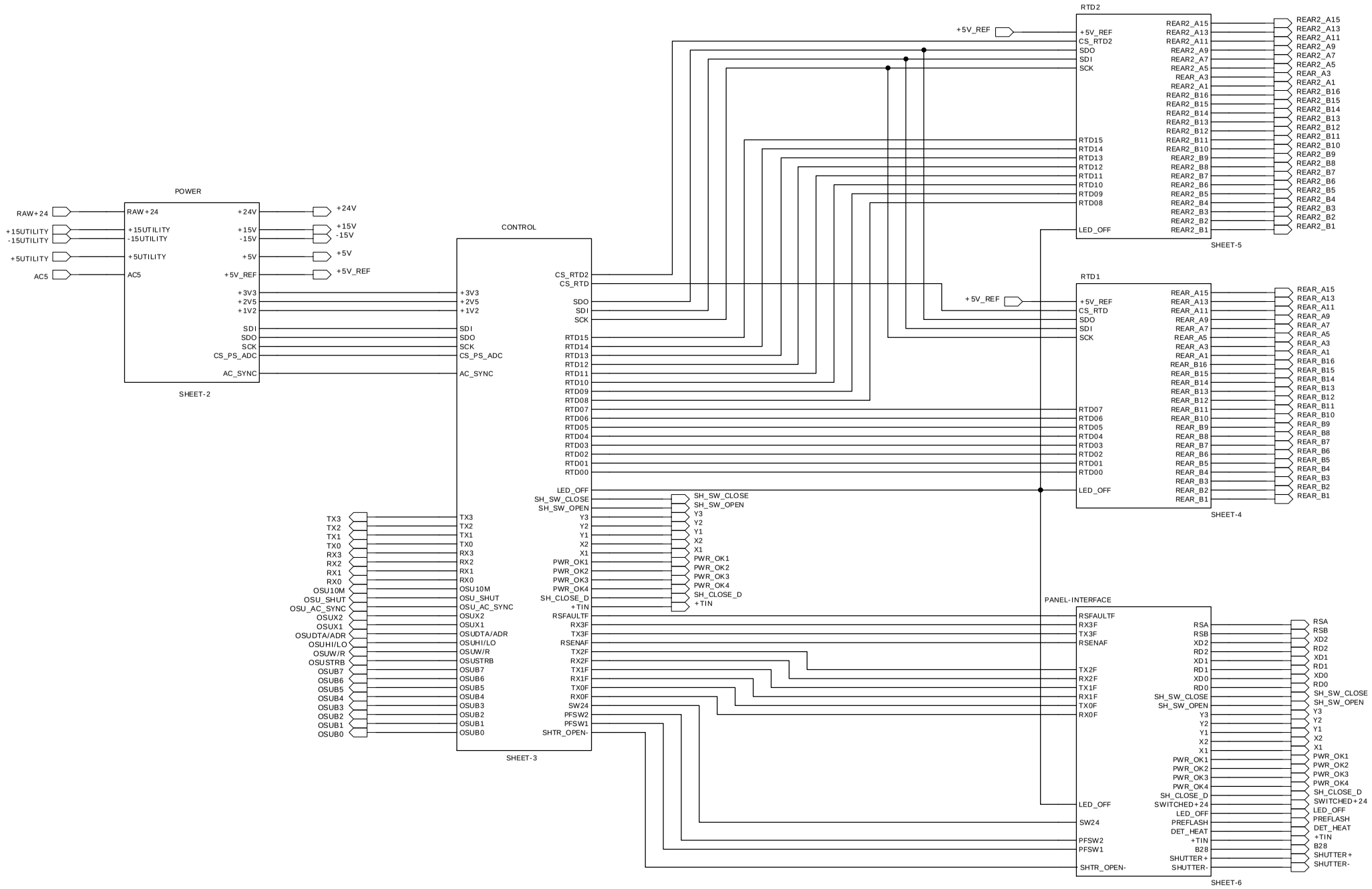




REVISION RECORD		

COMPANY: THE OHIO STATE UNIVERSITY DEPARTMENT OF ASTRONOMY IMAGING SCIENCES LABORATORY			
TITLE: PA-POWER			
DRAWN: moj	DATED: 12/10/2013		
CHECKED:	DATED:	CODE:	SIZE: C / DRAWING NO: KMT_PostAmp_Final.sch / REV: NR
QUALITY CONTROL:	DATED:		
RELEASED:	DATED:	SCALE: NONE	SHEET: 5 OF 5

REVISION RECORD		



COMPANY: THE OHIO STATE UNIVERSITY DEPARTMENT OF ASTRONOMY IMAGING SCIENCES LABORATORY					
TITLE: TOP					
DRAWN: MOJ/DPP	DATED: 3/12/2015	CODE:	SIZE: C	DRAWING NO: UtilityBoard_R2m.sch	REV: A
CHECKED:	DATED:	SCALE: NONE		SHEET: 1 OF 7	

6 5 4 3 2 1

REVISION RECORD		

J1
LS2-125-01-XX-D-RA1
-ADC7 ADC8
RAW+24 RAW+24
ADC9 -15UTILITY
-15UTILITY +15UTILITY
+15UTILITY +5UTILITY
+5UTILITY -ADC5
ADC3 ADC6
ADC4
AC5 AC5

+15 V for analog

+15UTILITY TP44 LT1085 VIN VOUT ADJ U1 TP41 +15V
C1 10m/35V
C3 0.1u/50V
C2 2.2uF/35V
C5 22uF/35V
R1 3.01k
RV1 1K
C4 10uF
C6 0.1u/50V
R2 38.3k
C7 10m/35V
C8 2.2uF/35V
R3 1.5k
C9 0.1u/50V
C10 2.2uF/35V
R4 3.32k
RV2 1K
C11 0.1u/50V
R5 20.0k
-15UTILITY TP43 LT1185 VIN VOUT REF GND FB U2 TP42 -15V

-15V for analog

+24 V for shutter, detector heat, serial, RTDs, LEDs

R159
RAW+24 TP45 UC3836 VIN ISENSE VOUT DRIVE COMP GND RGND SENS U3 Q1 TIP32B TP46 +24V
R38=40.2k for UC3836, 16.2k for UC3835
C13 0.1u/50V
C12 2.2uF/35V
C14 0.1u/50V
R6 40.2k
C15 22uF/35V
RV3 1K
C16 0.1u/50V
R7 4.22k

+5 AC for sync

TP49 AC5 R10 5.1k
C22 0.1u/50V
D1 1N914-SMD
D2 1N914-SMD
+3V3 R11 2.2k
+15V C23 0.1u/50V
C24 0.1u/50V
-15V
LM311N U5
AC_SYNC TP52

FPGA Supplies

+5V U6 VIN VOUT GND LD1117-3.3V TP32 +3V3
C115 0.1u/50V
C114 1u/25V
C116 0.1u/50V
C124 16V 10u
TP33

TP31 U32 VIN VOUT GND LD1117-2.5V +2V5
C121 0.1u/50V
C120 1u/25V
C122 0.1u/50V
C123 16V 10u

U31 VIN VOUT GND LD1117-1.2V TP24 +1V2
C118 0.1u/50V
C117 1u/25V
R12 120
C119 16V 10u
TP30

-ADC5 10.0k/1% R130 R30 +15V
OP-27 U20 TRIM1 TRIM2 V+ V- OUT ADC5
R131 4.99k/1% -15V

-ADC7 10.0k/1% R154 R132 +15V
OP-27 U41 TRIM1 TRIM2 V+ V- OUT ADC7
R155 4.99k/1% -15V

+5 V for this board

+5V
+5UTILITY TP47 LT1764A VIN VOUT SHDN GND ADJ U4 TP48 R8 14.3k
C17 10m/35V
C18 2.2uF/35V
C19 0.1u/50V
C20 2.2uF/35V
C21 0.1u/50V
RV4 1K
R9 4.22k
TP1 TP2 TP3 TP4 SCOPE_LOOP

U12 TP VIN NC GND TP NC VOUT TRIM ADR435
+15V C40 2.2uF/35V C41 0.1u/50V GND GND
TP51 +5V_REF C42 0.1u/50V GND C150 47uF/16V

-15V 100k/1% R37 10.0k/1% R39 +15V
OP-27 U11 TRIM1 TRIM2 V+ V- OUT
R38 9.09k/1% -15V
4.7k R40

10.0k/1% R13 +15V
OP-27 U40 TRIM1 TRIM2 V+ V- OUT
TP50 -5VREF
R16 4.99k/1% -15V 47uF/16V C151

TP54 10.0k/1% R157 10.0k/1% R156 +15V
OP-27 U42 TRIM1 TRIM2 V+ V- OUT TP53
R158 4.99k/1% -15V

+24V +15V +5V
R41 30.0k/1%
R45 191k/1%
R43 88.7k/1%
R42 10.0k/1%
R44 10.0k/1%
R46 10.0k/1%

J6-26 +TIN ADC3 ADC10
ADC4 ADC5 ADC1
J6-21 ADC6 ADC7 ADC8 ADC9
ADC2 J6-16
LTC2418 U10 CH0 CH1 CH2 CH3 CH4 CH5 CH6 CH7 CH8 CH9 CH10 CH11 CH12 CH13 CH14 CH15 COM
VCC REF+ REF- SDI SCK SDO CS FO NC1 NC2 GND
+5V_REF TP38 SDI TP39 SCK SDO TP40 CS_PS_ADC TP37
GND
+5V C43 10u/16V C44 0.1u/50V GND

DRAWN: MOJ/DPP	DATED: 3/12/2015	COMPANY: THE OHIO STATE UNIVERSITY DEPARTMENT OF ASTRONOMY IMAGING SCIENCES LABORATORY	
CHECKED:	DATED:	TITLE: POWER	
		CODE:	SIZE: C
		DRAWING NO: UtilityBoard_R2m.sch	REV: A
		SCALE: NONE	SHEET: 2 OF 7

6 5 4 3 2 1

D C B A

REVISION RECORD		

to MOTHERBOARD

HEADER-2X32-MOD-IV
J2

to RS-232

U30
EP3C16-PQFP240

to PANEL BOARD

1-Wire Serial Number

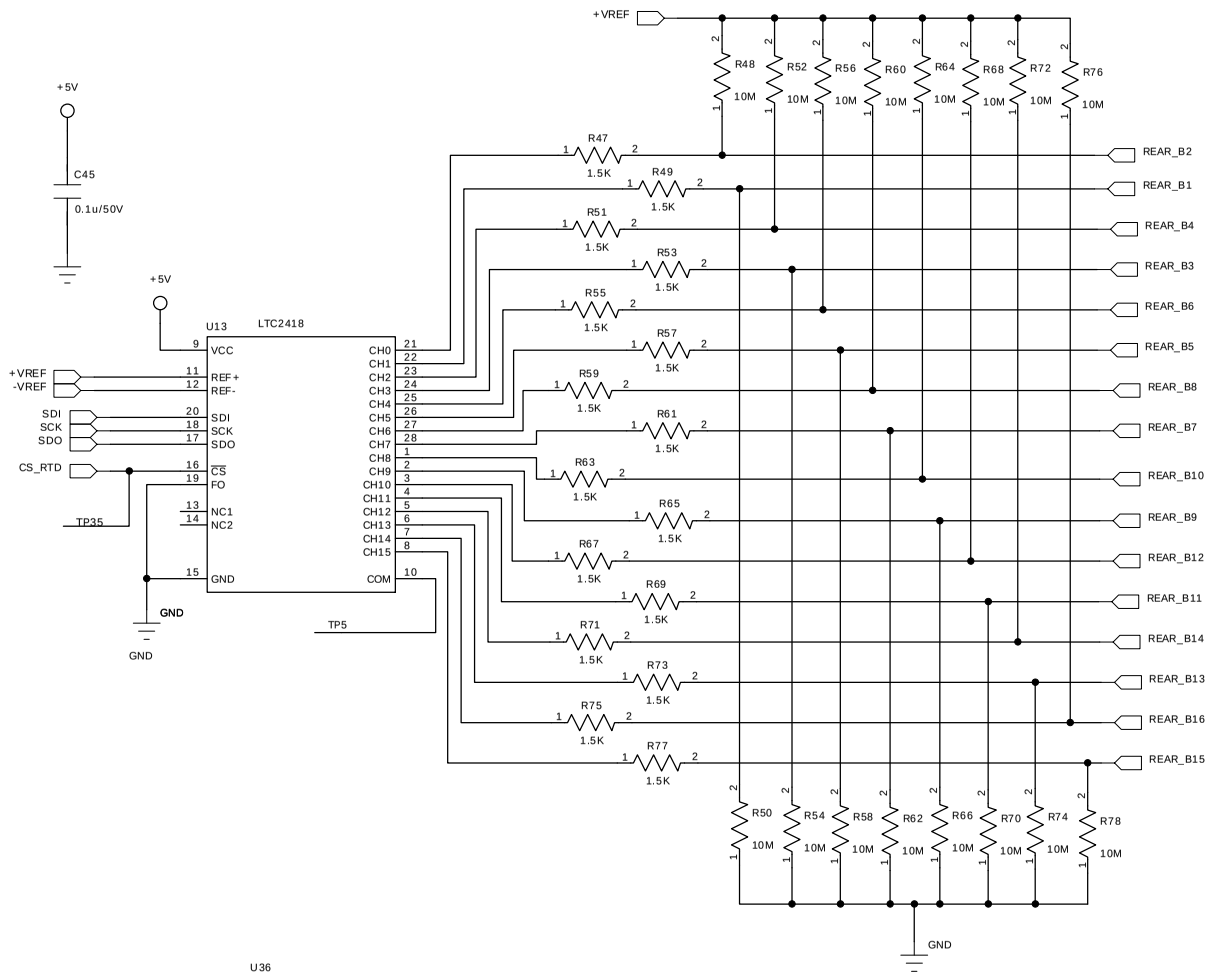
ALTERA_CONFIG
EPCS4
DS2401_TO92
DS2480B_8SOIC
SN74LVCH8T245
74LS04
XTAL_OSC

COMPANY:	THE OHIO STATE UNIVERSITY DEPARTMENT OF ASTRONOMY IMAGING SCIENCES LABORATORY		
TITLE:	CONTROL		
DRAWN: MOJ/DPP	DATED: 3/12/2015	CODE:	SIZE: C
CHECKED:	DATED:	DRAWING NO: UtilityBoard_R2m.sch	REV: A
SCALE: NONE		SHEET: 3 OF 7	

from Aluminizing:RTD Board:rtd7_final

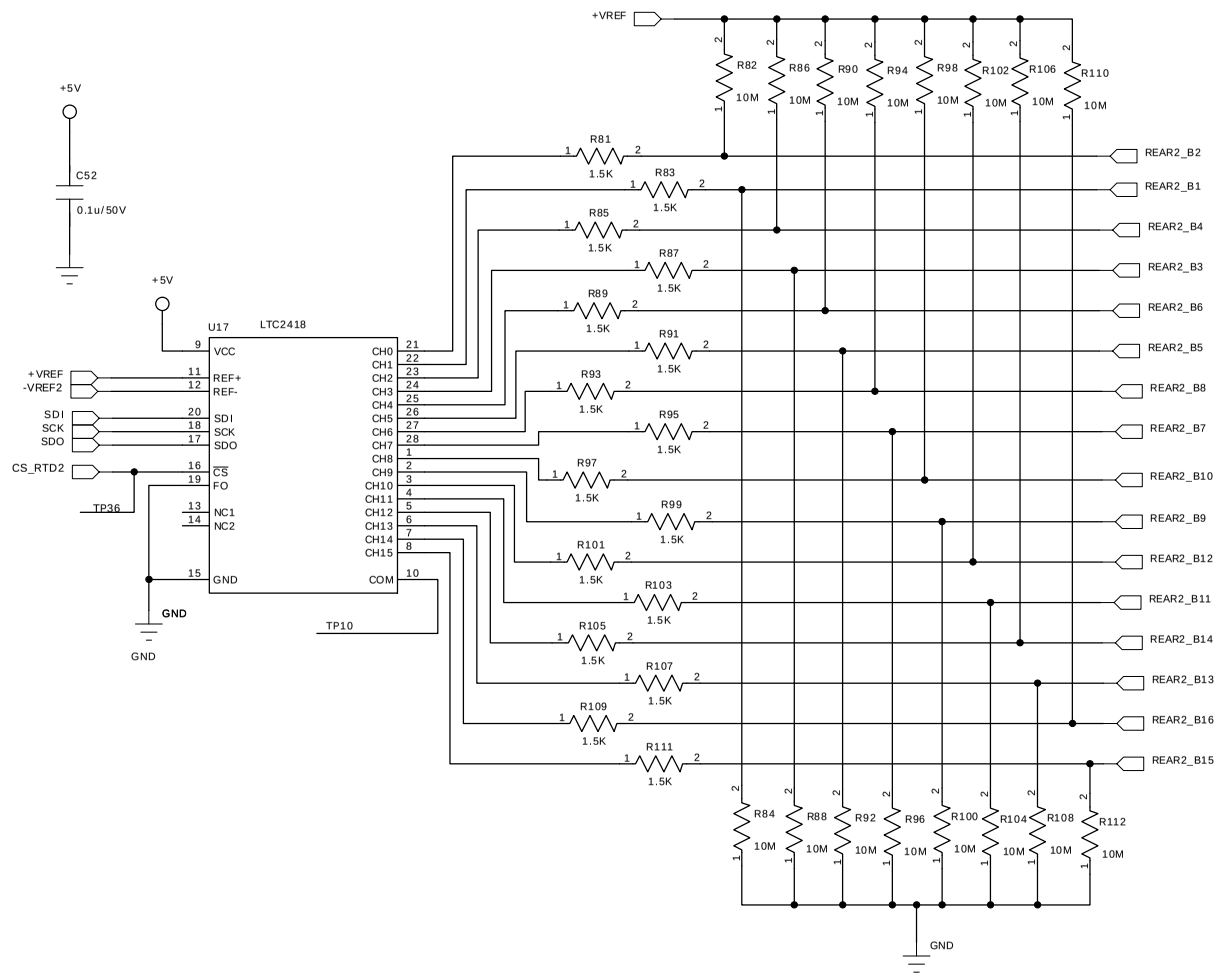
REVISION RECORD		

RTDs

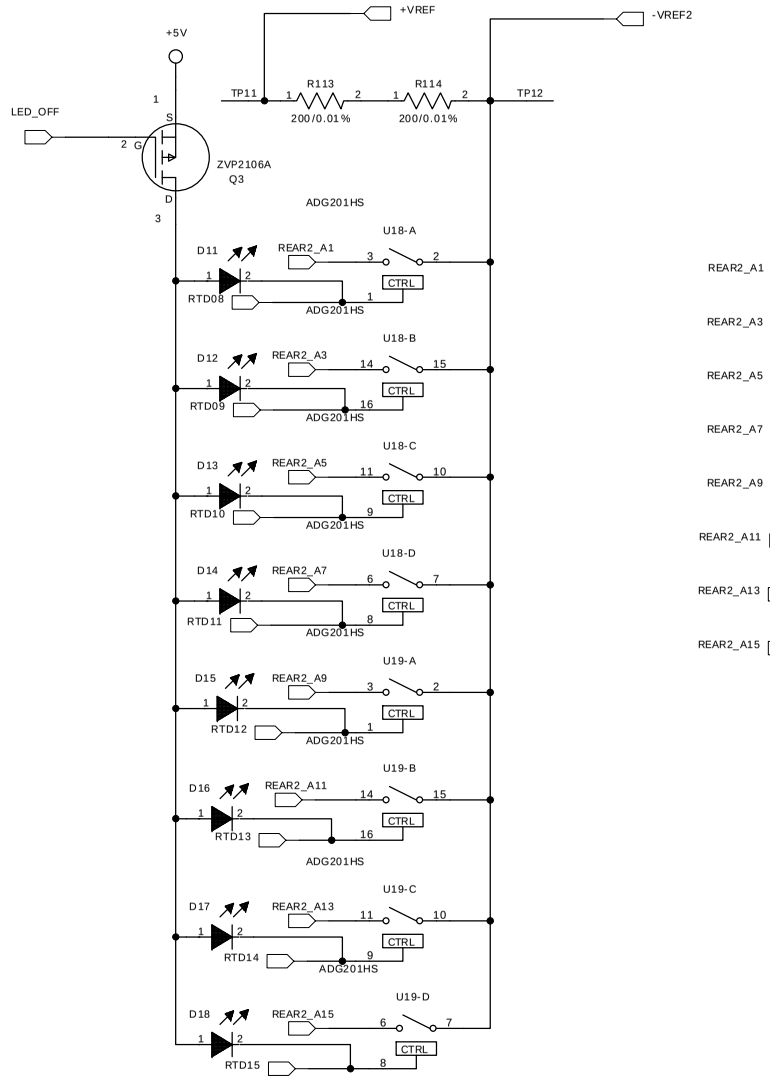


COMPANY: THE OHIO STATE UNIVERSITY DEPARTMENT OF ASTRONOMY IMAGING SCIENCES LABORATORY			
TITLE: RTD1			
DRAWN: MOJ/DPP	DATED: 3/12/2015	CODE:	SIZE: C
CHECKED:	DATED:	SCALE: NONE	DRAWING NO: UtilityBoard_R2m.sch
			REV: A
			SHEET: 4 OF 7

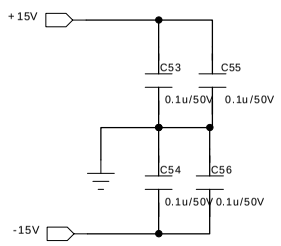
REVISION RECORD		

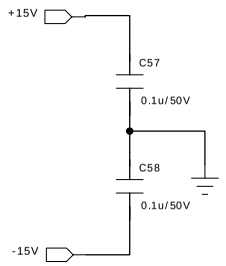


from Aluminizing:RTD Board:rtd7_final



RTDs

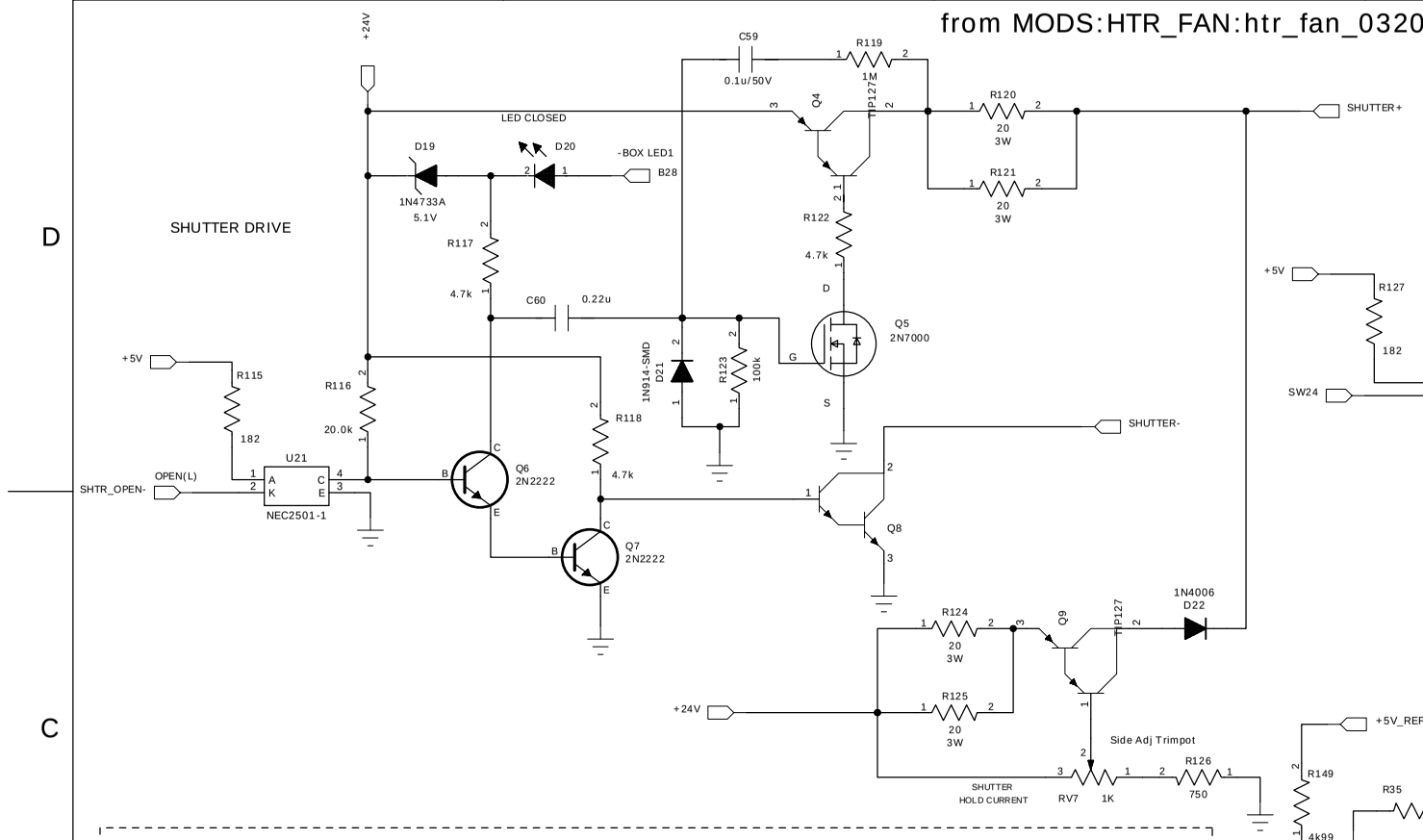




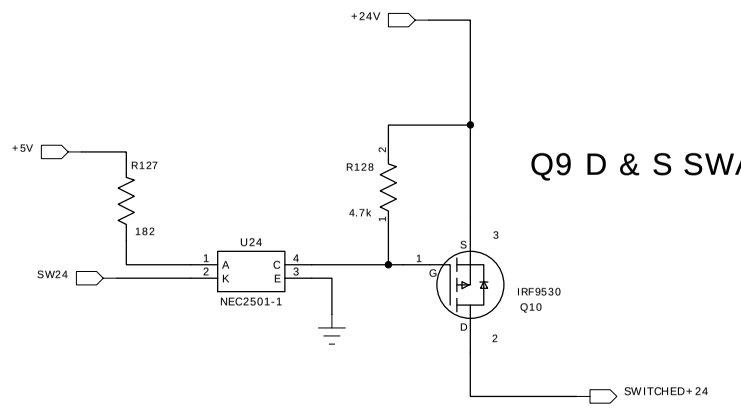
COMPANY: THE OHIO STATE UNIVERSITY DEPARTMENT OF ASTRONOMY IMAGING SCIENCES LABORATORY					
TITLE: RTD2					
DRAWN: MOJ/DPP	DATED: 3/12/2015	CODE:	SIZE: C	DRAWING NO: UtilityBoard_R2m.sch	REV: A
CHECKED:	DATED:	SCALE: NONE		SHEET: 5 OF 7	

from MODS:HTR_FAN:htr_fan_03202007

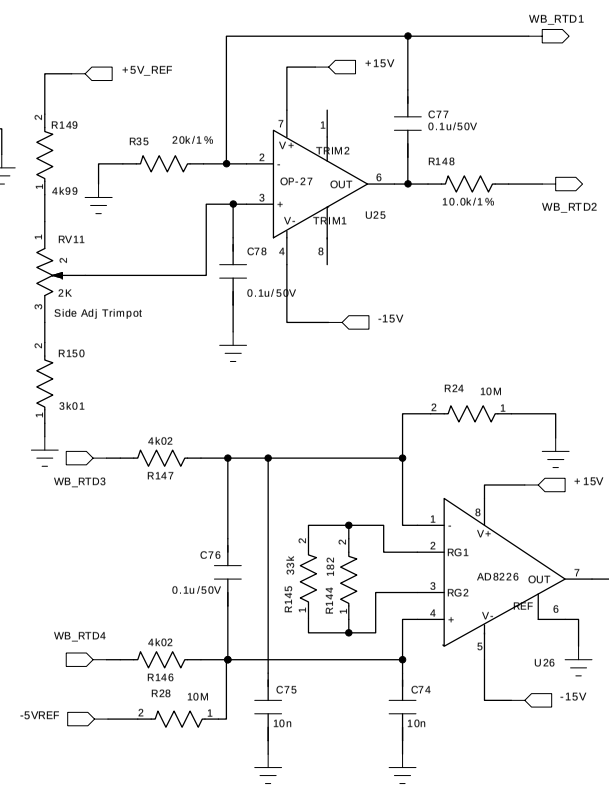
SHUTTER DRIVE



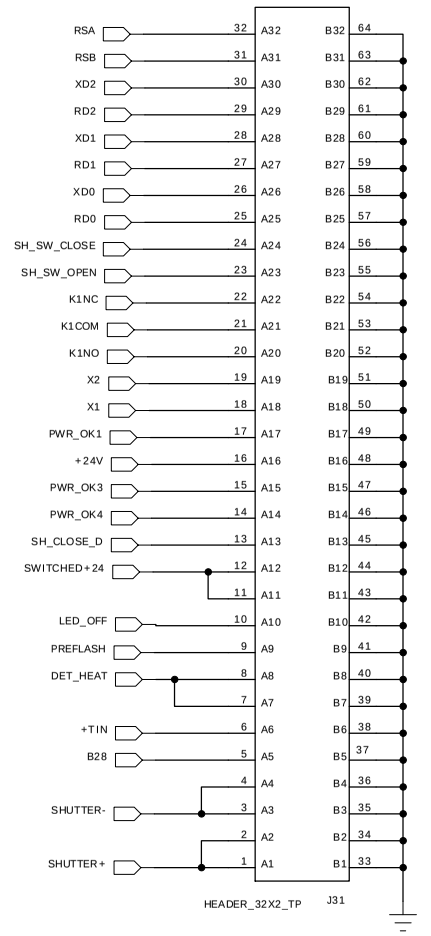
Q9 D & S SWAPPED from V2



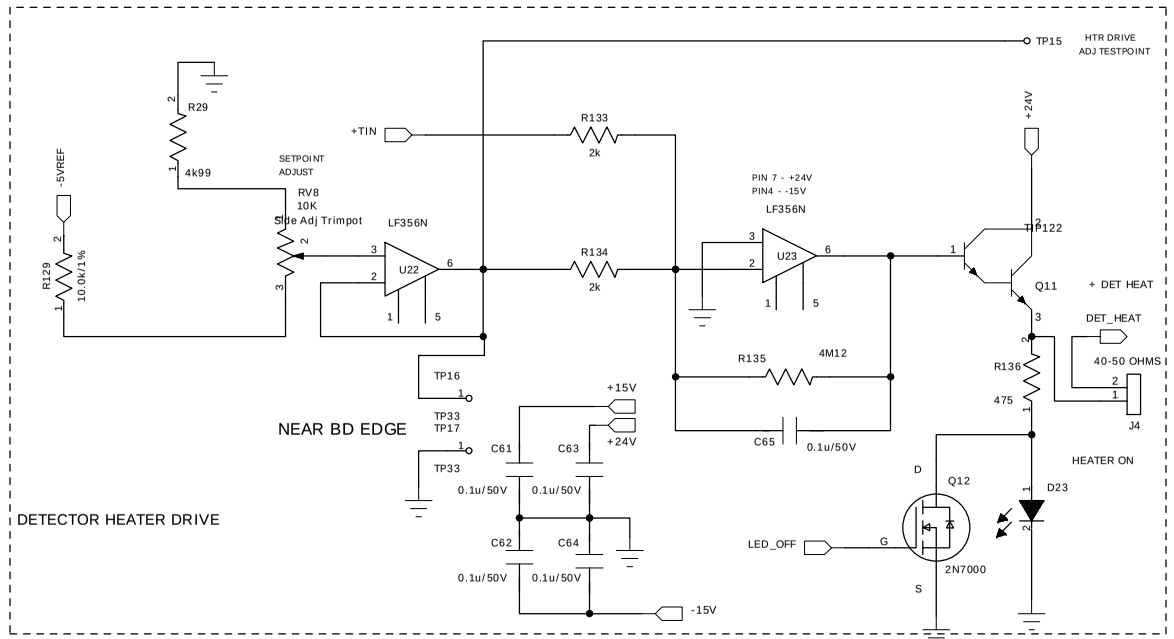
100 uA source



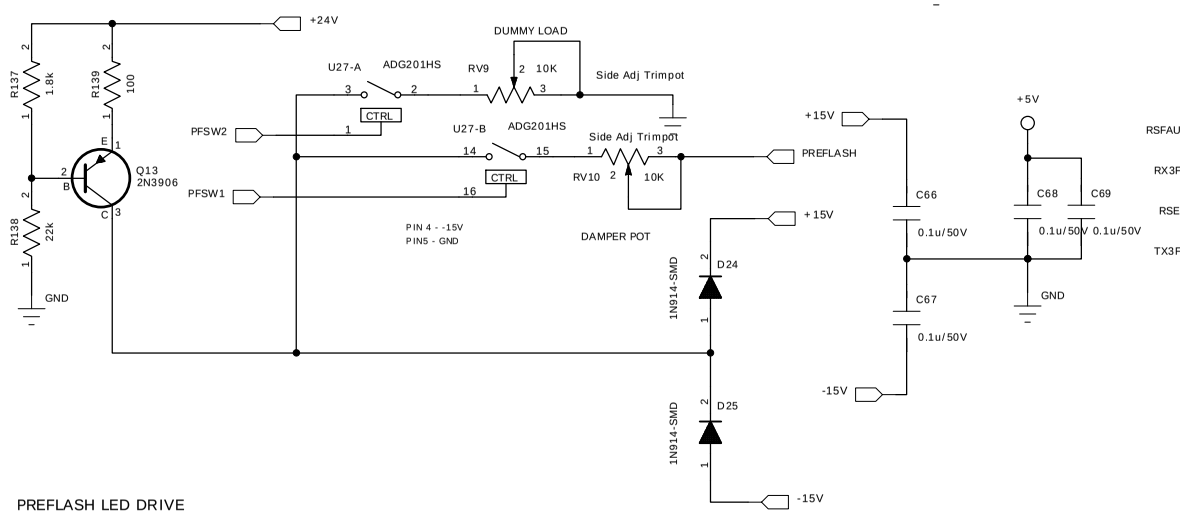
TO FRONT PANEL



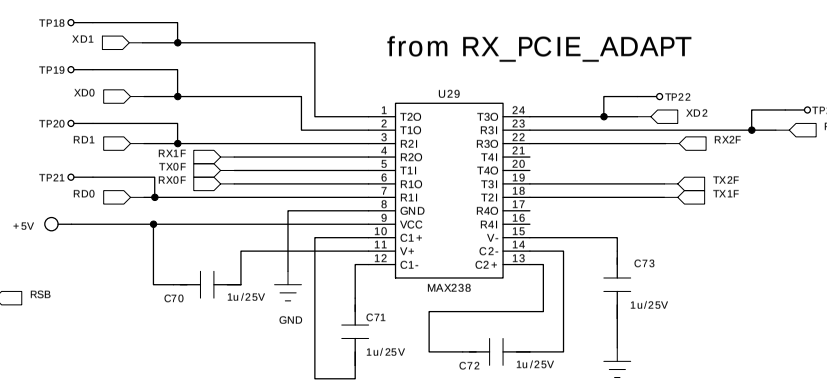
NEAR BD EDGE

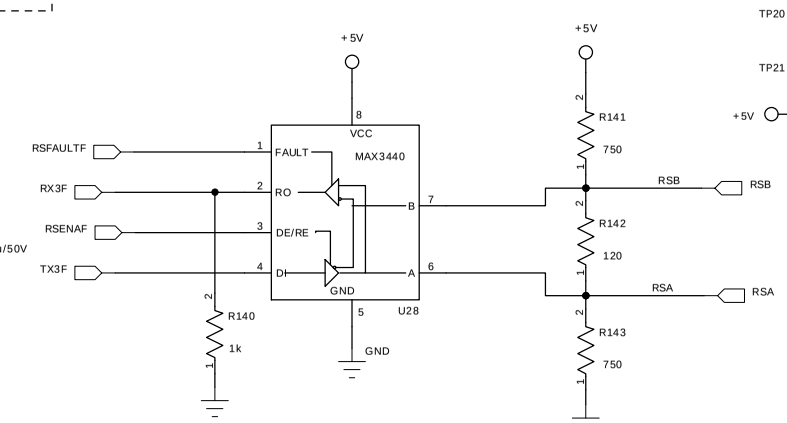


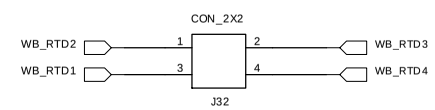
PREFLASH LED DRIVE

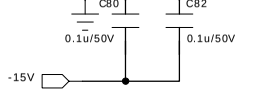


from RX_PCIE_ADAPT





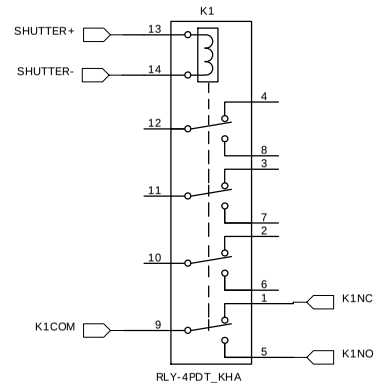


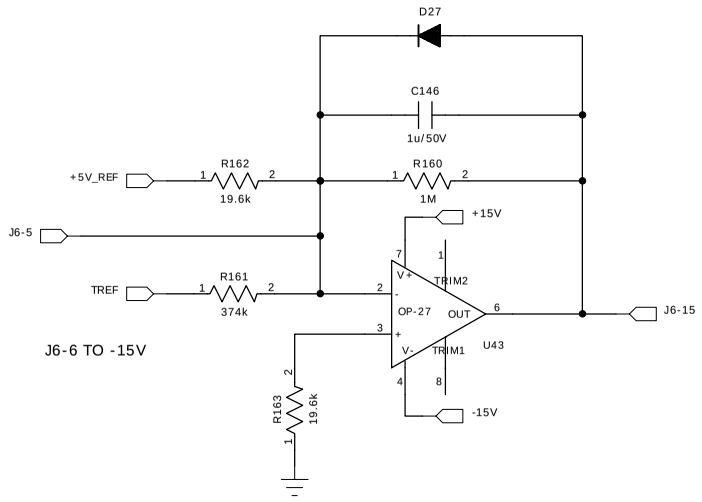


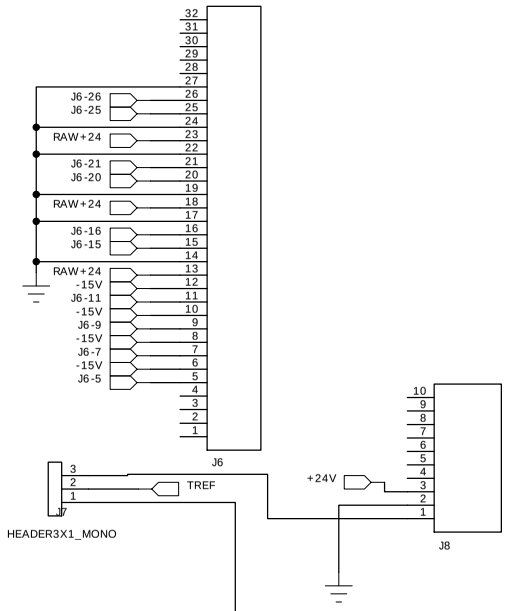
REVISION RECORD		

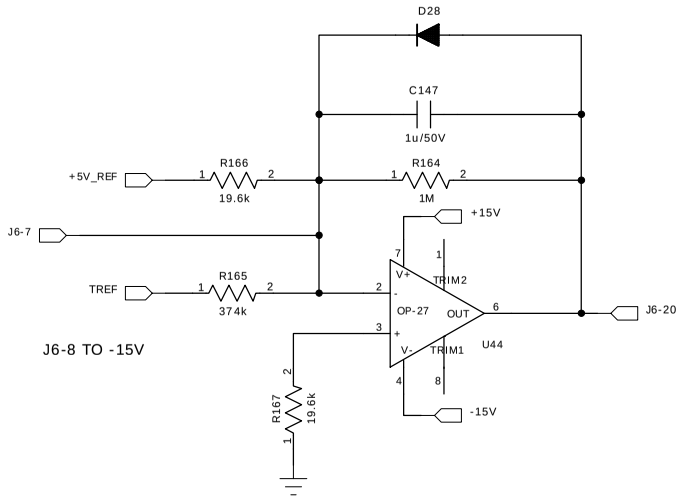
COMPANY: THE OHIO STATE UNIVERSITY DEPARTMENT OF ASTRONOMY IMAGING SCIENCES LABORATORY					
TITLE: PANEL-INTERFACE					
DRAWN: MOJ/DPP	DATED: 3/12/2015	CODE:	SIZE: C	DRAWING NO: UtilityBoard_R2m.sch	REV: A
CHECKED:	DATED:	SCALE: NONE		SHEET: 6 OF 7	

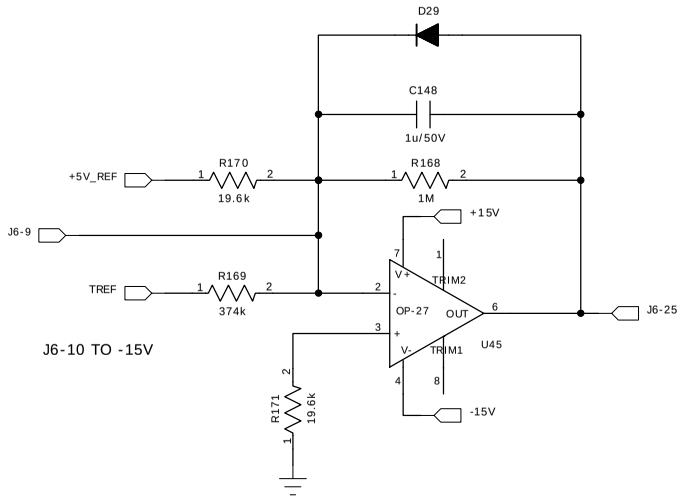
REVISION RECORD		

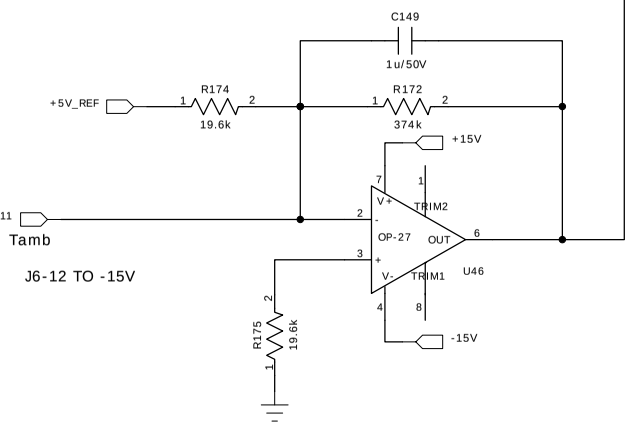


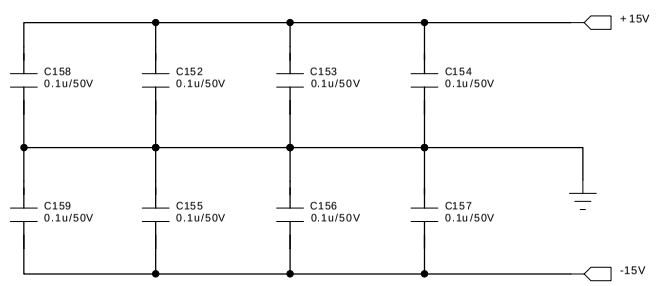




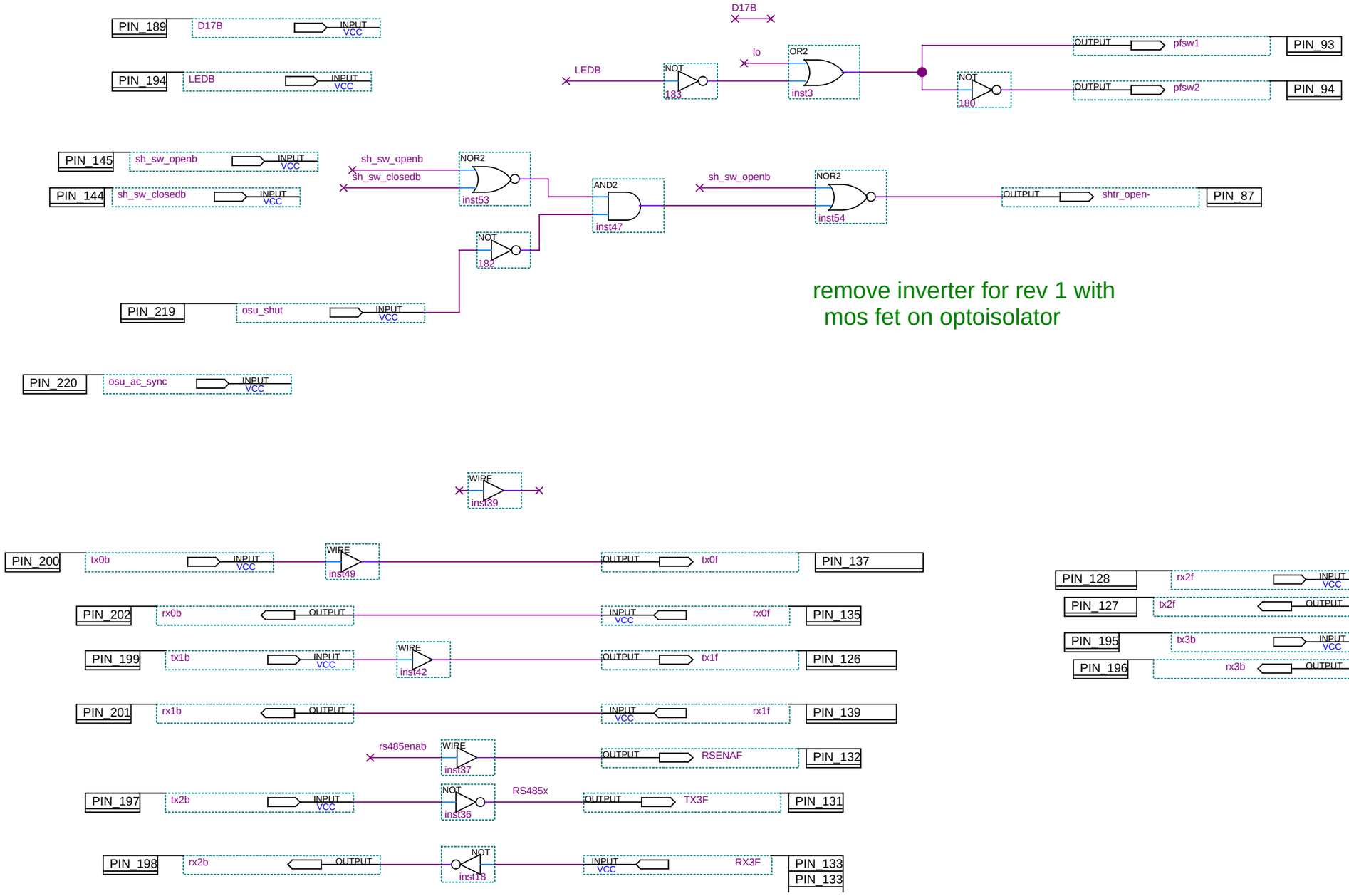


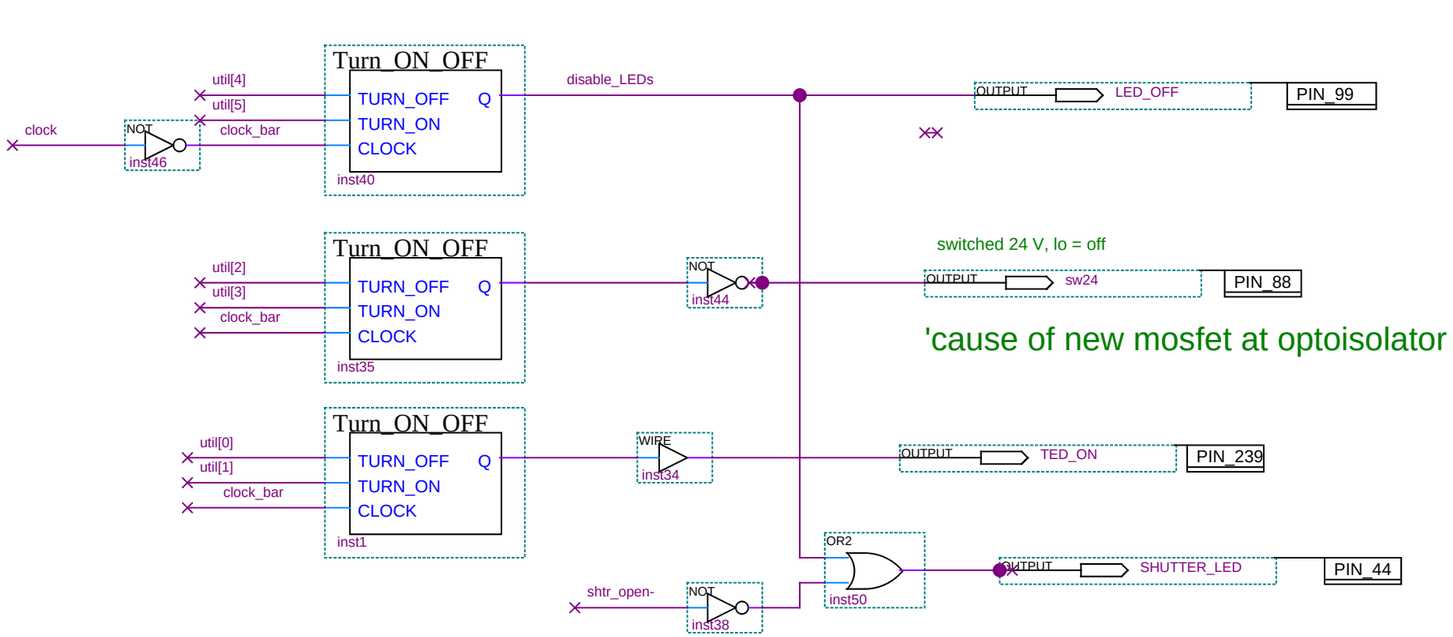


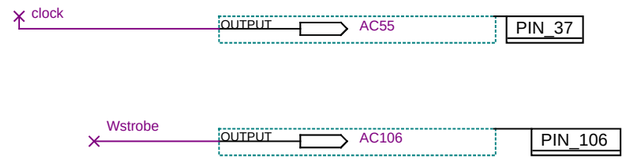


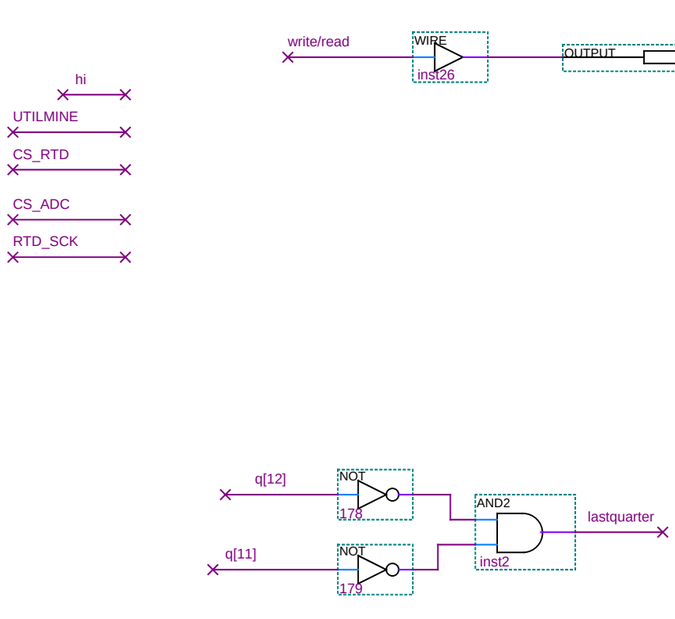


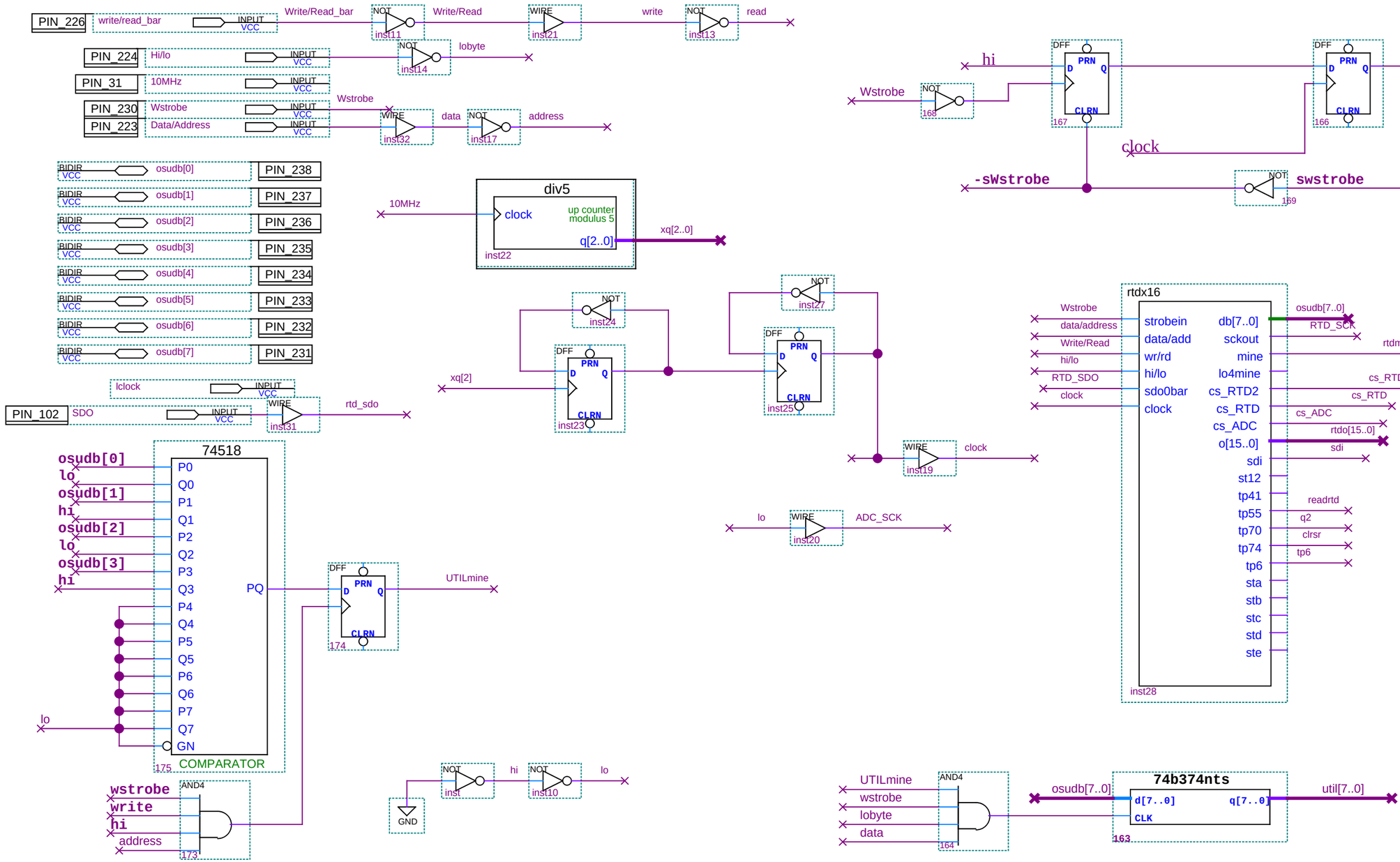
COMPANY: THE OHIO STATE UNIVERSITY DEPARTMENT OF ASTRONOMY IMAGING SCIENCES LABORATORY					
TITLE: BOG+RELAY					
DRAWN: MOJ/DPP	DATED: 3/12/2015	CODE:	SIZE: C	DRAWING NO: UtilityBoard_R2m.sch	REV: A
CHECKED:	DATED:	SCALE: NONE		SHEET: 7 OF 7	

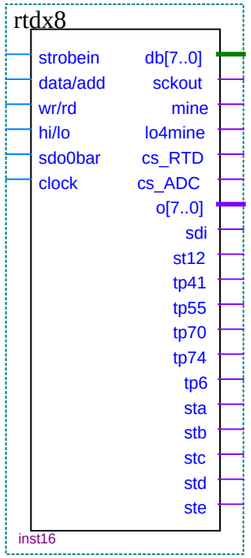

PIN_189
D17B
INPUT
VCC
PIN_194
LEDB
INPUT
VCC
D17B
lo
LEDB
NOT
183
OR2
inst3
NOT
180
OUTPUT
pfsw1
PIN_93
OUTPUT
pfsw2
PIN_94
PIN_145
sh_sw_openb
INPUT
VCC
PIN_144
sh_sw_closedb
INPUT
VCC
sh_sw_openb
sh_sw_closedb
NOR2
inst53
AND2
inst47
sh_sw_openb
NOR2
inst54
OUTPUT
shtr_open-
PIN_87
NOT
182
PIN_219
osu_shut
INPUT
VCC
remove inverter for rev 1 with
mos fet on optoisolator
PIN_220
osu_ac_sync
INPUT
VCC
WIRE
inst39
PIN_200
tx0b
INPUT
VCC
WIRE
inst49
OUTPUT
tx0f
PIN_137
PIN_202
rx0b
OUTPUT
INPUT
VCC
rx0f
PIN_135
PIN_199
tx1b
INPUT
VCC
WIRE
inst42
OUTPUT
tx1f
PIN_126
PIN_201
rx1b
OUTPUT
INPUT
VCC
rx1f
PIN_139
rs485enab
WIRE
inst37
OUTPUT
RSENAF
PIN_132
PIN_197
tx2b
INPUT
VCC
NOT
inst36
RS485x
OUTPUT
TX3F
PIN_131
PIN_198
rx2b
OUTPUT
NOT
inst18
INPUT
VCC
RX3F
PIN_133
PIN_133
PIN_128
rx2f
INPUT
VCC
PIN_127
tx2f
OUTPUT
PIN_195
tx3b
INPUT
VCC
PIN_196
rx3b
OUTPUT


Turn_ON_OFF
util[4]
util[5]
clock_bar
clock
NOT
inst46
TURN_OFF
TURN_ON
CLOCK
Q
inst40
disable_LEDs
OUTPUT
LED_OFF
PIN_99
Turn_ON_OFF
util[2]
util[3]
clock_bar
inst35
NOT
inst44
switched 24 V, lo = off
sw24
PIN_88
'cause of new mosfet at optoisolator
Turn_ON_OFF
util[0]
util[1]
clock_bar
inst1
WIRE
inst34
TED_ON
PIN_239
OR2
inst50
shtr_open-
inst38
SHUTTER_LED
PIN_44

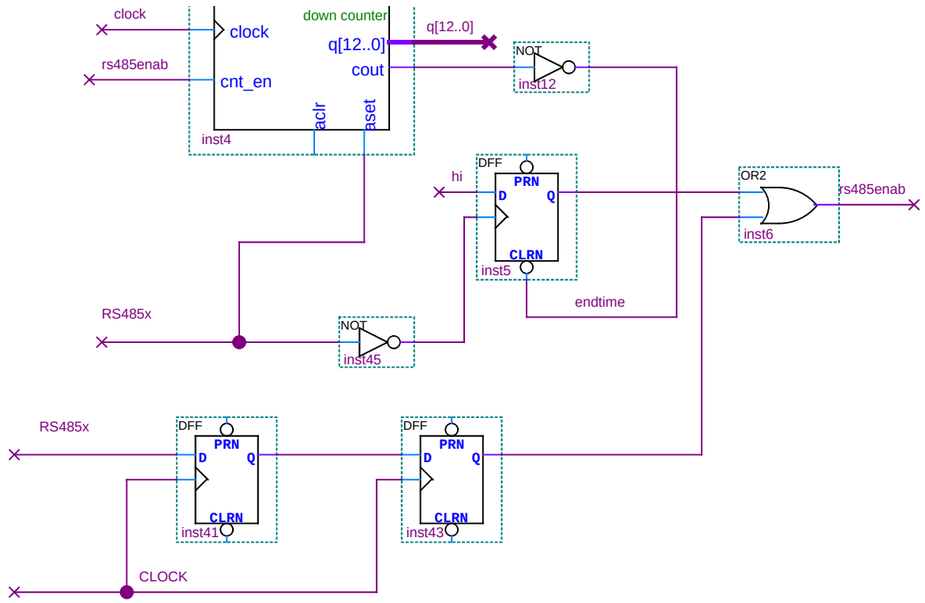

clock
OUTPUT
AC55
PIN_37
Wstrobe
AC106
PIN_106
rtdmine
AC112
PIN_112
RTD_SCK
AC114
PIN_114


write/read
WIRE
inst26
w/r
PIN_222
hi
UTILMINE
CS_RTD
CS_ADC
RTD_SCK
cs_rtd
rtd_sck
readrtd
sdi
rtd_sdo
osudb[7]
data
write
q[12]
q[11]
NOT
179
AND2
inst2
lastquarter
lo
osudb[6]
osudb[5]
cs_adc
osudb[0]
ac18
PIN_86
osudb[1]
ac1
PIN_183
osudb[2]
ac2
PIN_181
osudb[3]
ac15
PIN_185
osudb[4]
ac25
PIN_187
osudb[5]
ac64
PIN_203
osudb[6]
AC120
PIN_120
ac29
osudb[7]
AC118
PIN_118
ac28
lobyte
AC110
PIN_110
ac24
wstrobe
AC108
ac22

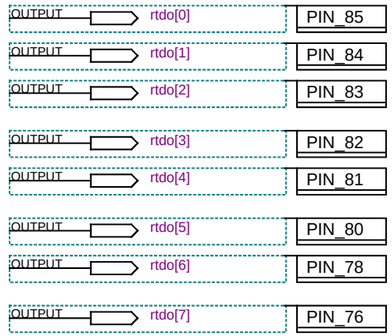

PIN_226
write/read_bar
INPUT
VCC
Write/Read_bar
NOT
inst11
Write/Read
WIRE
inst21
write
NOT
inst13
read
PIN_224
Hi/lo
NOT
inst14
lobyte
PIN_31
10MHz
Wstrobe
PIN_230
PIN_223
Data/Address
WIRE
inst32
data
NOT
inst17
address
BIDIR
osudb[0]
PIN_238
osudb[1]
PIN_237
osudb[2]
PIN_236
osudb[3]
PIN_235
osudb[4]
PIN_234
osudb[5]
PIN_233
osudb[6]
PIN_232
osudb[7]
PIN_231
lclock
PIN_102
SDO
rtd_sdo
inst31
div5
clock
up counter
modulus 5
q[2..0]
inst22
xq[2..0]
xq[2]
NOT
inst24
DFF
PRN
D
Q
CLRN
inst23
NOT
inst27
inst25
74518
osudb[0]
lo
osudb[1]
hi
osudb[2]
lo
osudb[3]
hi
P0
Q0
P1
Q1
P2
Q2
P3
Q3
P4
Q4
P5
Q5
P6
Q6
P7
Q7
GN
PQ
COMPARATOR
175
lo
wstrobe
write
hi
address
AND4
173
UTILmine
174
NOT
inst
hi
NOT
inst10
lo
GND
hi
Wstrobe
NOT
168
DFF
167
clock
-sWstrobe
NOT
169
swstrobe
166
WIRE
inst19
clock
lo
WIRE
inst20
ADC_SCK
rtdx16
Wstrobe
data/address
Write/Read
hi/lo
RTD_SDO
clock
strobein
data/add
wr/rd
hi/lo
sdo0bar
clock
db[7..0]
sckout
mine
lo4mine
cs_RTD2
cs_RTD
cs_ADC
o[15..0]
sdi
st12
tp41
tp55
tp70
tp74
tp6
sta
stb
stc
std
ste
osudb[7..0]
RTD_SCK
rtdmine
cs_RTD2
cs_RTD
cs_ADC
rtdo[15..0]
sdi
readrtd
q2
clrsr
tp6
inst28
UTILmine
wstrobe
lobyte
data
AND4
164
osudb[7..0]
74b374nts
d[7..0]
q[7..0]
CLK
163
util[7..0]

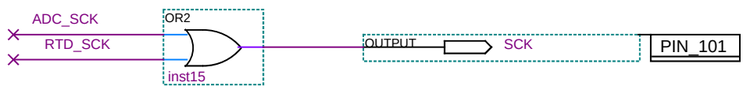


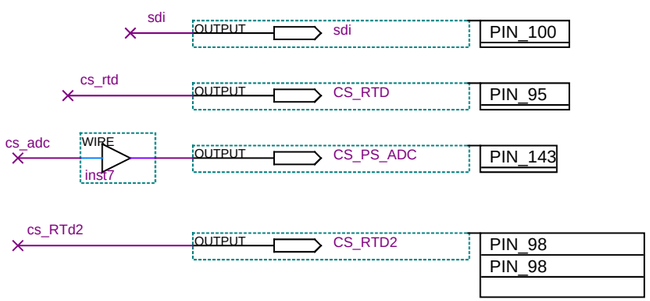
1600 micro sec retrigerable one-shot
holds rs485 bus in transmit for 1600 microsec after
last transmit transition or about 1.5 characters

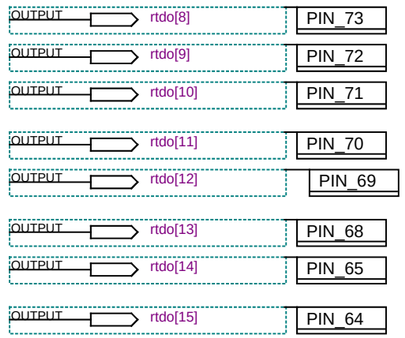


delays turn off via serial data to remove glitch as timer starts









TITLE	ROSMOS HE Power Supply (MK II)		
COMPANY	OSU ISL		
DESIGNER	Bruce		
NUMBER	1.00	REV	A
DATE	Wed Apr 01 16:03:40 2015	SHEET 1 OF	1

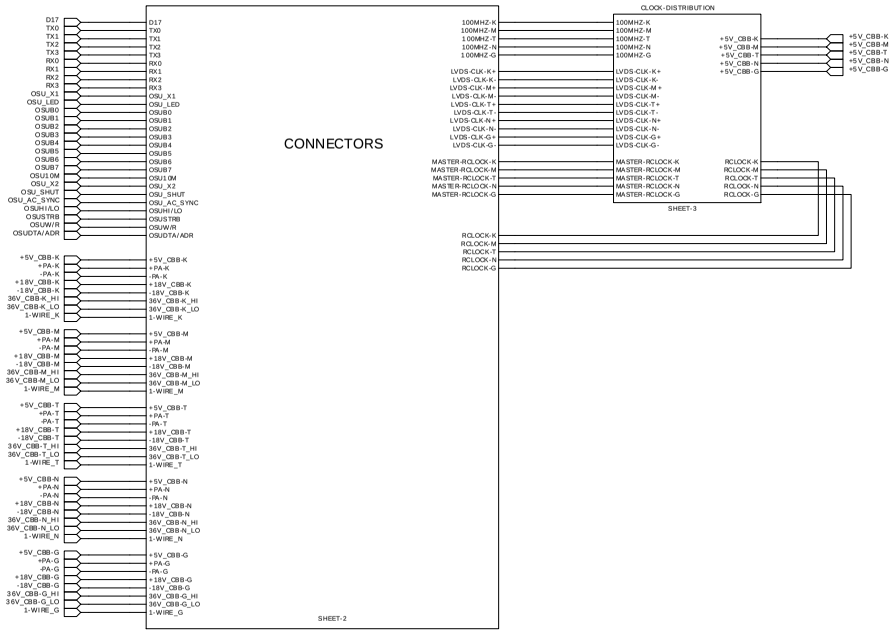
Utility Board Checkout

1. Set RV1 full CW before powering up (+15 may be too high otherwise)
2. Check R79+80 (TP6&7) and R113+114 (TP11&12) both should be 400+/- 0.06 Ohms
3. Install jumper on J4
4. Place Board to be tested on bracket, connect the cable to Cap board, NO others yet
5. +15 Volt supply won't go to 15, 15.5V is ok TP 41
6. -15 Volt supply RV2, TP42
7. +24 Volt supply, RV3, TP 46
8. +5 Volt supply, RV4, TP 48
9. +3.3 Volt supply, fixed, TP 32
10. +2.5 Volt supply, fixed TP 31
11. +1.2 Volt supply. Foxed TP 24 on solder side
12. +/- 5 Volt Ref TP 51/51
13. AC Sync signal, line freq ~square wave, TP 52
14. BGA
    a. Oscillator
    b. Level shifters
    c. Front panel buffers
    d. Config
15. Set RTD Vref, Rv5, (TP6 or 11) to 1 volt
16. DMP heater/RTD circuit and heater driver
    a. With 100 ohm 0.01% reisistor adjust RV11 for 2.7315 volts at +Tin (J31, front panel connector, pin 6) (this gets the system gain correct 10mv/K at 0 C)
    b. Connect pot and adjust for 1.5 volts at +Tin (150K, a good set point for DMP)
    c. Adjust RV8, set point, for LED 23, D23 ~ ½ on (led off bit must be off)
17. Power off, mount in box, connect mother board , front panel WB blue RTD, and BOG cables
18. Voltage ADC unity-gain invertors for negative voltages. Utility board must be directly connected to Cap board for raw voltages. Cap board must have divider resistors. Dan will provide a cable, someday, to use the service bracket. Check LED off bit,
19. Serial number and one-wire driver
20. RTD 1, santec blue cable between J5 and wallboard, RTDs 1 to 8
21. RTD 2, 2 x 16 header J30, RTDs 9 to 16, don't confuse with BOG 2 x 16 header
22. MicroIon+ interface, RS485 buffer and switched +24
23. Shutter solenoid driver, test with switch and program (shutter timer program)
24. Preflash driver, set RV9 and RV10 full CCW, check for 10 ma (KMTN data program with NFLASH=10000
25. RS232 Driver, UART0
26. Bog heater ckts (3)
    a. U43
    b. U44
    c. U45
27. Board s/n =

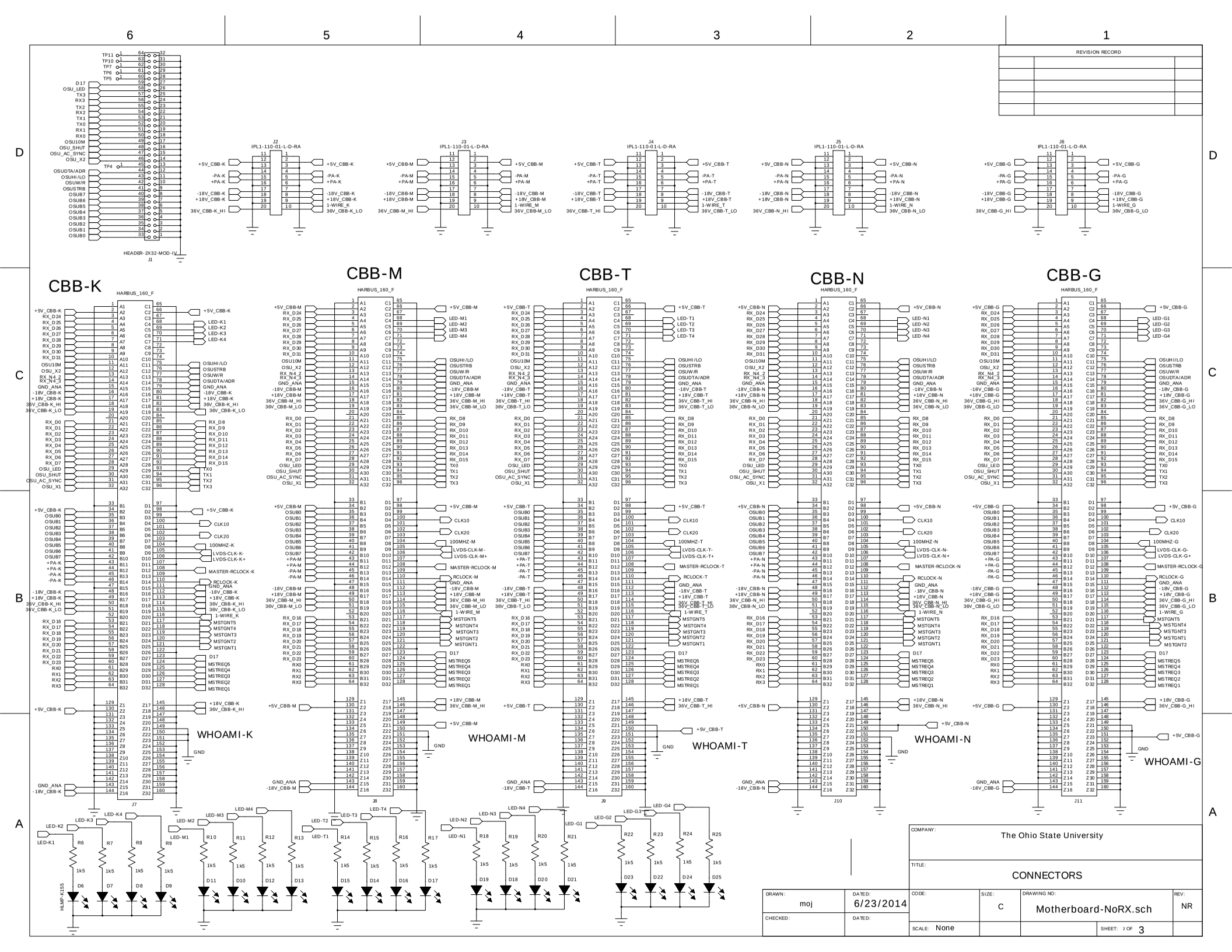
28. Date=

29. By whom=

REVISION RECORD		



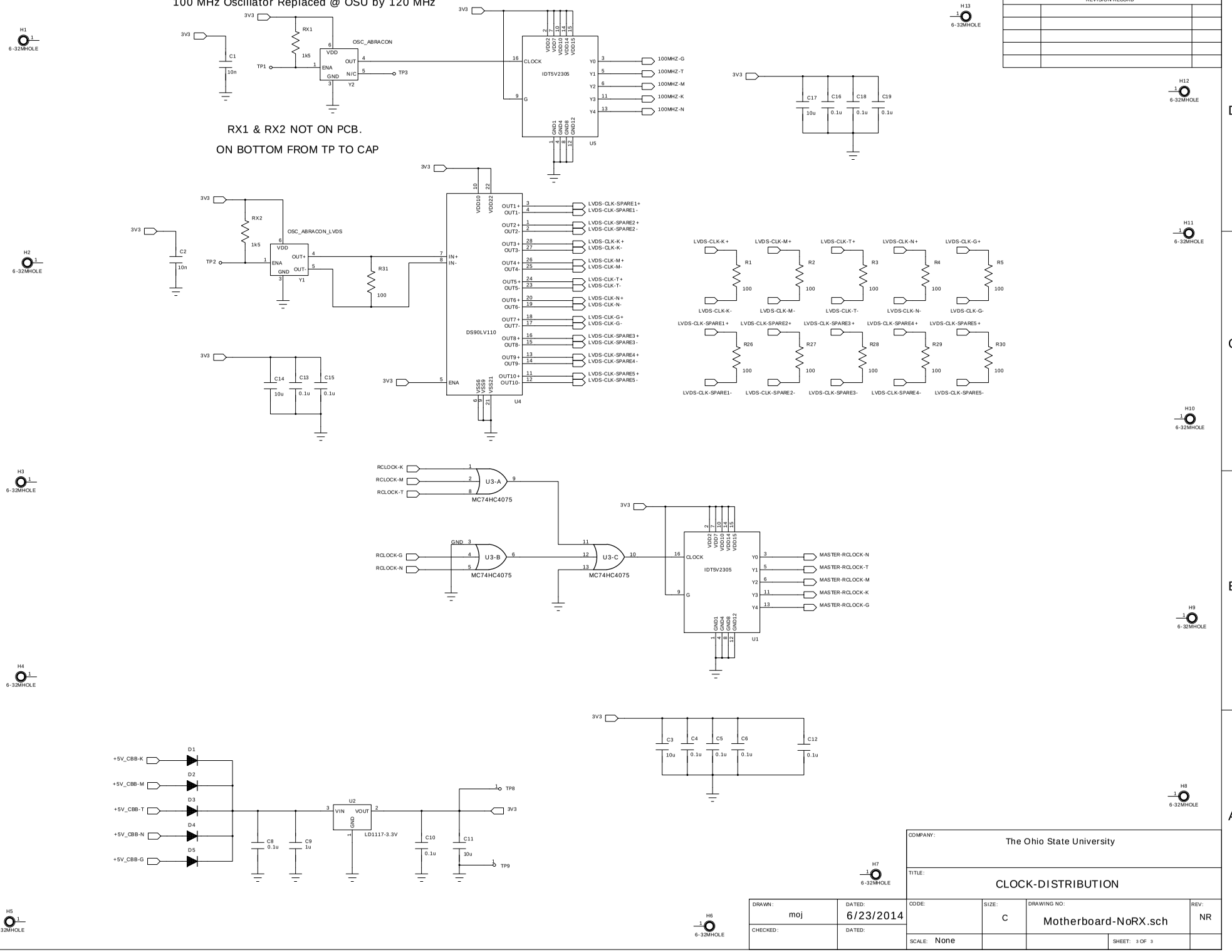
DRAWN: moj	DATED: 8/16/2011	COMPANY: The Ohio State University				
		TITLE: Samtec Crosstalk Test Board				
CHECKED:	DATED:	CODE:	SIZE: C	DRAWING NO.: Samtec Crosstalk Test		REV: NR
		SCALE: None			SHEET: 1 OF 3	


REVISION RECORD
CBB-K
CBB-M
CBB-T
CBB-N
CBB-G
WHOAMI-K
WHOAMI-M
WHOAMI-T
WHOAMI-N
WHOAMI-G
HARBUS_160_F
HEADER-2X32-MOD-IV
IPL1-110-01-L-D-RA
COMPANY: The Ohio State University
TITLE: CONNECTORS
DRAWN: moj
DATED: 6/23/2014
CHECKED:
DATED:
CODE:
SIZE: C
DRAWING NO: Motherboard-NoRX.sch
REV: NR
SCALE: None
SHEET: 2 OF 3

100 MHz Oscillator Replaced @ OSU by 120 MHz

RX1 & RX2 NOT ON PCB.

ON BOTTOM FROM TP TO CAP



COMPANY:	The Ohio State University
TITLE:	CLOCK-DISTRIBUTION
DRAWN: moj	DATED: 6/23/2014
CHECKED:	DATED:
CODE:	SIZE: C
DRAWING NO:	Motherboard-NoRX.sch
REV:	NR
SCALE: None	SHEET: 3 OF 3

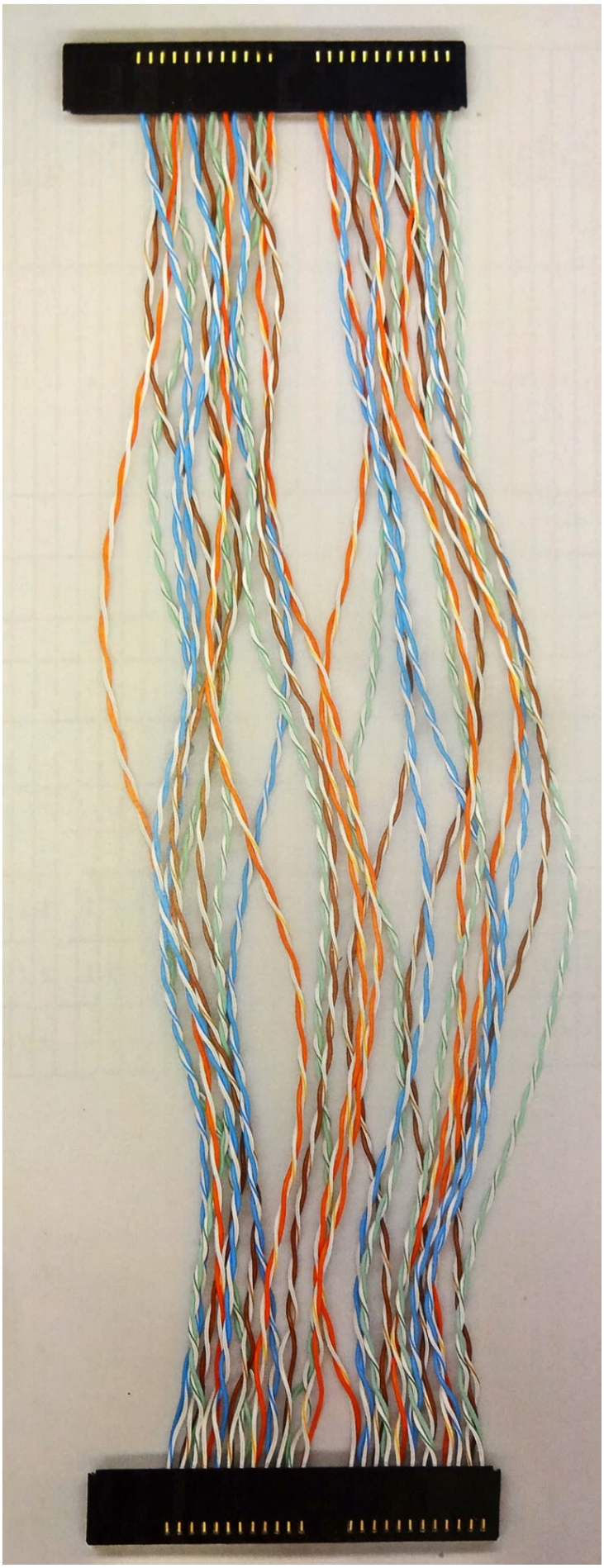
1. Cables from the Regulator Boards to the Mother Board (5) are:
Samtec MMSD-10-20-L-28.00-D-K-LDX.

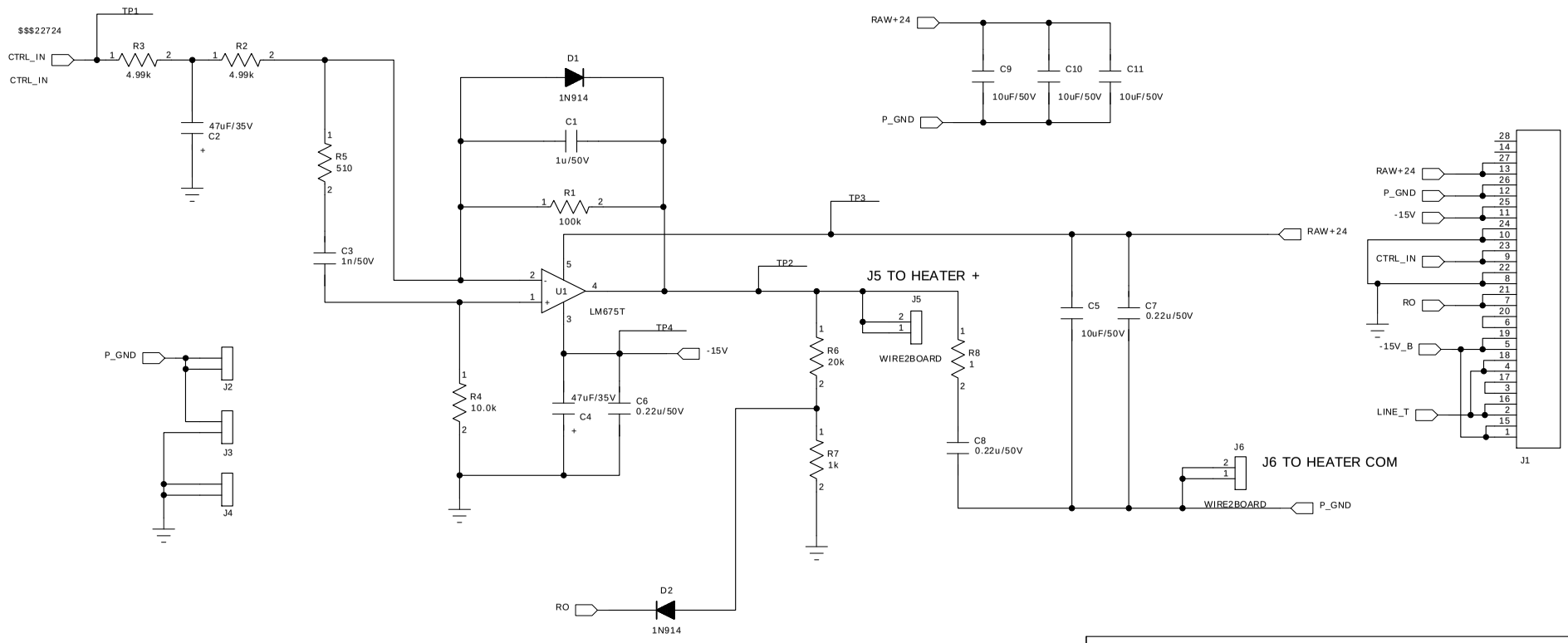
These are 20 conductor assemblies wired with AWG 20.

2.

Cable from the Mother Board to the Utility Board is terminated each end with 32x2 MOD IV with polarizing tab and end features for retainer/ejectors. Pins 1 to 12 and 16 to 27 are wire d 1:1 with twisted pairs from cat-5 wire. The returns are on the pins across, that is 33 to 44 and 48 to 59. See the photo.

System Wiring List											
Instrument Name: KMT Camera system	Cable Desc.: HE internal wiring from Util Bd to HE panel										
Instrument Name: KMT Camera system	Component No.: 210										
Instrument Name: KMT Camera system	Connector Length. 52"										
Instrument Name: KMT Camera system	64-pin (2X32) Header										
Instrument Name: KMT Camera system	9-pin CPC Series 2 Panel Male										
Instrument Name: KMT Camera system	RJ45 (T568A) Panel Jack (wire colors won't match T568A)										
Instrument Name: KMT Camera system	RJ13 Panel Jack										
Instrument Name: KMT Camera system	8-pin CPC Series 2 Panel Female										
Instrument Name: KMT Camera system	4-pin (2X2) ISL standard RTD Header										
Signal Name	64-pin	9-pin CPC Ser 2	RJ45	RJ13	4-pin RTD	5X2 Mod 4 Relay	8-pin CPC Ser 2	Wire Color	Wire Type	Wire AWG/ Note	Signal Type
Shut +	1	8						GRN	soft	24	
Shut +	2					4		ORG	soft	24	
Shut -	3	7						YEL	soft	24	
Shut -	4					5		BRN	soft	24	
Preflash LED	9	1						WHT	soft	24	
GND	42	2						PUR	soft	24	
Relay Com	21	4				1		BLK	soft	24	
Relay NC	22	5				2		RED	soft	24	
Relay NO	20	6				3		BLU	soft	24	
Switched +24	11		BLU/WHT					BLU/WHT	cat 5 pair	with 43	
GND	43		BLU					BLU	cat 5 pair	with 11	
Switched +24	12		ORG/WHT					GRN/WHT	cat 5 pair	with 44	
GND	44		ORG					GRN	cat 5 pair	with 12	
RSB	31		GRN/WHT					ORG/WHT	cat 5 pair	with 32	
RSA	32		GRN					ORG	cat 5 pair	with 31	
GND	25			4 B/W				BLU/WHT	cat 5 pair	with 25	
RD0	57			5 O				BLU	cat 5 pair	with 57	
XD0	26			3 B				BRN/WHT	cat 5 pair	with 58	
GND	58			2 O/W				BRN	cat 5 pair	with 26	
RTD V+					1		1	BRN	soft	24	
RTD V-					3		2	RED	soft	24	
RTD I+					4		3	ORG	soft	24	
RTD I-					2		4	YEL	soft	24	
Det_Heat	8						5	GRY	soft	24	
GND	40						6	PUR	soft	24	
SH_SW_OPEN	23							RED	soft	24	
SH_SW_CLOSED	24							ORG	soft	24	
GND	56							BRN	soft	24	
+T_IN	6							TAN	soft		
GND	38							PNK	soft		





REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

COMPANY:
THE OHIO STATE UNIVERSITY
DEPARTMENT OF ASTRONOMY
IMAGING SCIENCES LABORATORY

TITLE:
KMT Boil Off Gas Heater Bd

CODE:	SIZE:	DRAWING NO:	REV:
	B	KMT BOG_Heat_f.sch	A

DRAWN:	DATED:	SCALE: NONE	SHEET: 1 OF 1
DPP	4/3/2015		

conduc number	body	1st band	2nd band	PT30 #1	PT30#2	PT13	function	cpc 28 pin		Utility BD J6	
1	Black			11			Raw24	1		23	
2	White			10			pwr gnd	2		24	
3	Red			9			-15	3		32	
4	Green			8			signal gnd	4		27	
5	Orange			7			drive	5		25	
6	Blue			6			nu	6		29	
7	White	Black		5			read bk	7		26	
8	Red	Black		4			nu			31	
9	Green	Black		3			-15	8		10	
10	Orange	Black		2			line temp	9		9	
11	Blue	Black			11		Raw24	10		18	
12	Black	White			10		pwr gnd	11		19	
13	Red	White			9		-15	12		30	
14	Green	White			8		signal gnd	13		22	
15	Blue	White			7		drive	14		20	
16	Black	Red			6		nu	15		4	
17	White	Red			5		read bk	16		21	
18	Orange	Red			4		nu			3	
19	Blue	Red			3		-15	17		8	
20	Red	Green			2		Line temp	18		7	
21	Orange	Green				11	Raw24	19		13	
22	Black	White	Red			10	pwr gnd	20		14	
23	White	Black	Red			9	-15	21		28	
24	Red	Black	White			8	signal gnd	22		17	
25	Green	Black	White			7	drive	23		15	
26	Orange	Black	White			6	nu	24		2	
27	Blue	Black	White			5	read bk	25		16	
28	Black	Red	Green			4	nu	28		1	
29	White	Red	Green			3	-15	26		6	
30	Red	Black	Green			2	Line temp	27		5	
							Amb temp			11	
							-15			12	

back view (wire side)
of a 2 x 16 MOD IV as marked
and J1 of BOG heater driver PC Board

16	32
15	31
14	30
13	29
12	28
11	27
10	26
9	25
8	24
7	23
6	22
5	21
4	20
3	19
2	18
1	17

J6 pins layout , (as seen on component si
of Utility board.

32	31
30	29
28	27
26	25
24	23
22	21
20	19
18	17
16	15
14	13
12	11
10	9
8	7
6	5
4	3
2	1

BOG Internal cable goes from Utility board J6 to CPC 28 pin on HE front panel.
BOG External cable goes from HE CPC 28 pin to three 2 x 12 pin MOD IV female labled PT30#1, PT30#2 and PT13 above.
An additional 2 x 12 MOD IV female is on a short pig-tail to connect the second BOG driver board on each copper clam shell.

BOG Heater wiring, HE Internal and HE to BOG Driver Boards

de)

REVISION RECORD		

X21
MHOLE166

J7
QFSS-026-01-X-D-A-X

RTD1I-
RTD1I+
RTD2I-
RTD2I+
RTD3I-
RTD3I+
RTD4I-
RTD4I+
RTD5I-
RTD5I+
RTD6I-
RTD6I+
RTD7I-
RTD7I+
RTD8I-
RTD8I+
GND
RTD1V+
RTD1V-
RTD2V+
RTD2V-
RTD3V+
RTD3V-
RTD4V+
RTD4V-
RTD5V+
RTD5V-
RTD6V+
RTD6V-
RTD7V+
RTD7V-
RTD8V+
RTD8V-
RTD-GND

X22
MHOLE166

CON_2X16 J1

CON_2X2
CON1
CON2

CON_2X3
CON3
RTD9I-
HTR1A
RTD9I+
RTD9V+
HTR1B
RTD9V-

TP37
TP38
TP39
TP40
TP41
SIG-GND-G

O-RING-GROUND
TP33
TP34
TP35
TP36

HOL21
HOL22
HOL23
HOL24
HOL25
HOL26
HOL33
DH4MMP
HOLE3/8INCH

J172
DB-9
HTR2A
HTR2B
RTD9I-
HTR1A
RTD9I+
RTD9V+
HTR1B
RTD9V-

CAN BE STRAPPED TO EARTH GND

O-RING-GROUND

Outer Circle
Vacuum Flange bolt holes
HOL2164
HOL7489
HOL7157
HOL2171
HOL472
HOL798
HOL8009
HOL5542
DH3_048MMP

HOL1818
HOL6704
DH12_7MMN

Middle Circle (larger holes)
access holes for Mid Ring Bolts
HOL750
HOL1539
HOL1098
HOL1422
HOL9232
HOL4975
DH12_7MMN

vent screen mounting holes
HOL27
HOL29
HOL28
HOL30
DH3_175MMP

TP29
TP30
TP31
TP32
HTR2A
HTR2B

lifting eyes
HOL8538
HOL6038
HOL3622
HOL1
HOL31
HOL32
CHGND
DH4_2MMN

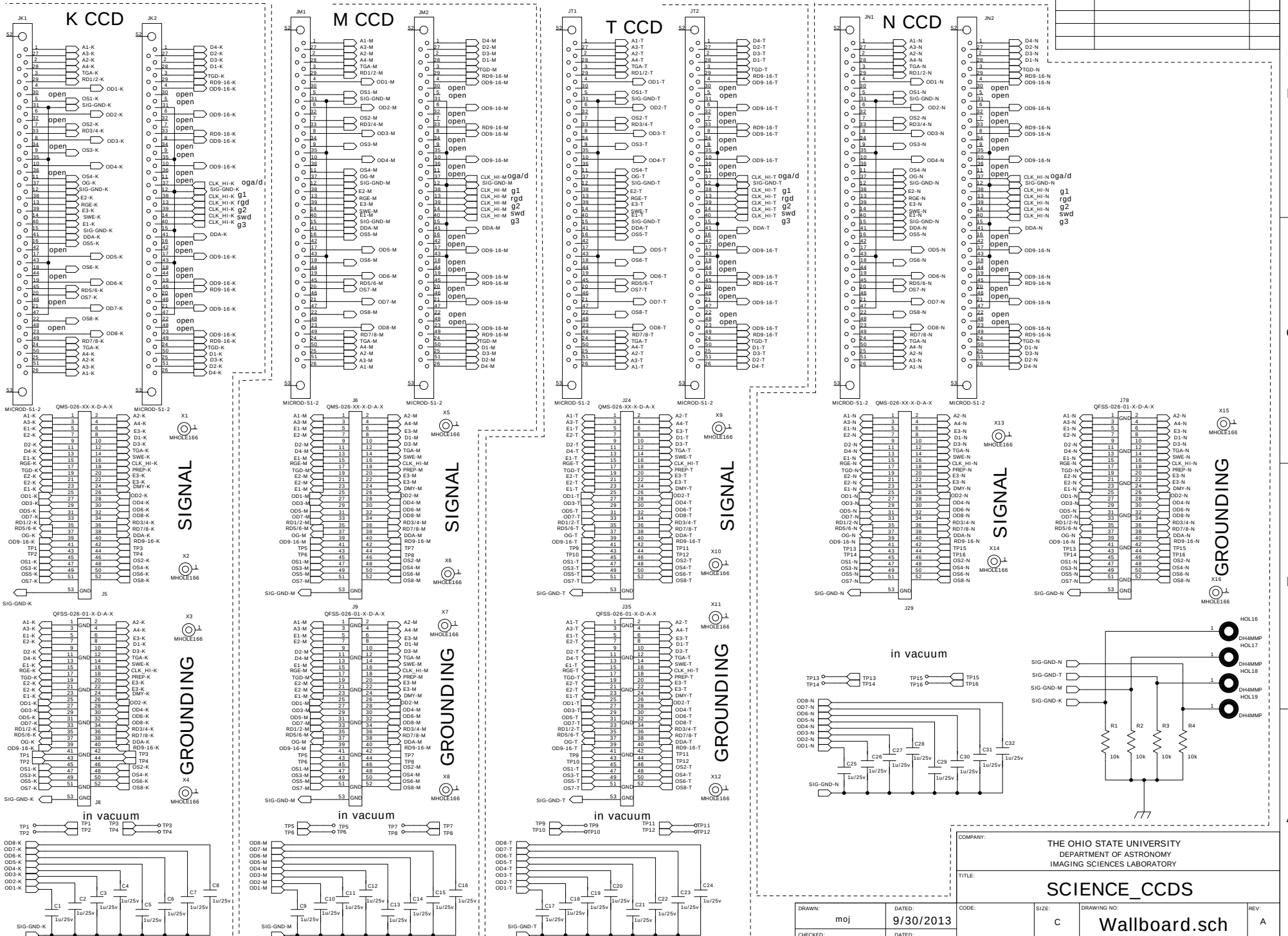
mid ring shoulder bolt holes
HOL1221
HOL5706
HOL2663
HOL2363
DH6_2MMN

Samtec cover mounting
HOL11
HOL13
HOL3
HOL5
HOL7
HOL9
HOL15
HOL10
HOL12
HOL2
HOL4
HOL6
HOL8
HOL14
DH3_048MMP

COMPANY:	THE OHIO STATE UNIVERSITY DEPARTMENT OF ASTRONOMY IMAGING SCIENCES LABORATORY				
TITLE:	MOUNT+RTDS				
DRAWN: moj	DATED: 9/30/2013	CODE:	SIZE: C	DRAWING NO: Wallboard.sch	REV: A
CHECKED:	DATED:	SCALE: NONE		SHEET: 1 OF 3	

A1-4: Image Area A Clocks OS1-8: Output Sources DOS1-8: Dummy Outputs TGA: Image Area A Transfer Gate SS: Substrate

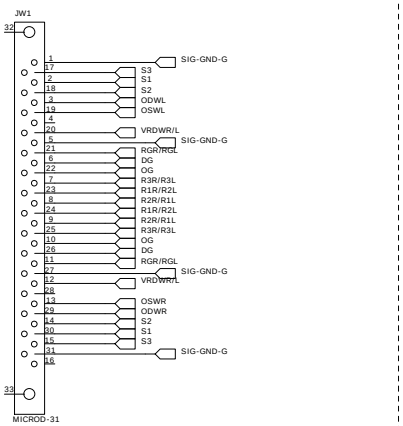
REVISION RECORD		



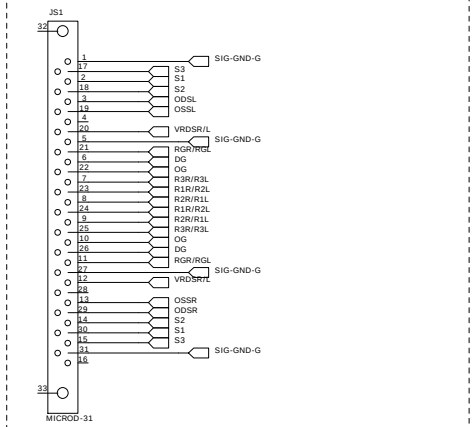
COMPANY:	THE OHIO STATE UNIVERSITY DEPARTMENT OF ASTRONOMY IMAGING SCIENCES LABORATORY		
TITLE:	SCIENCE_CCDS		
DRAWN: moj	DATED: 9/30/2013	CODE:	SIZE: C
CHECKED:	DATED:	SCALE: NONE	DRAWING NO: Wallboard.sch
			REV: A
			SHEET: 2 OF 3

REVISION RECORD		

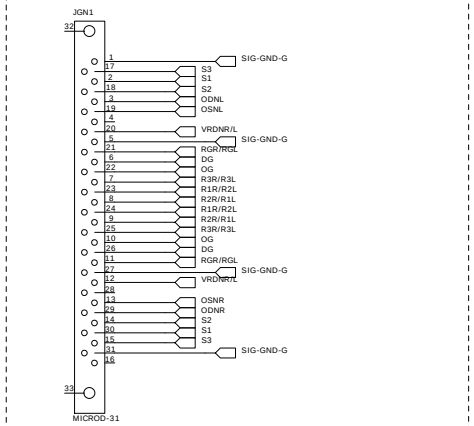
GUIDE WEST



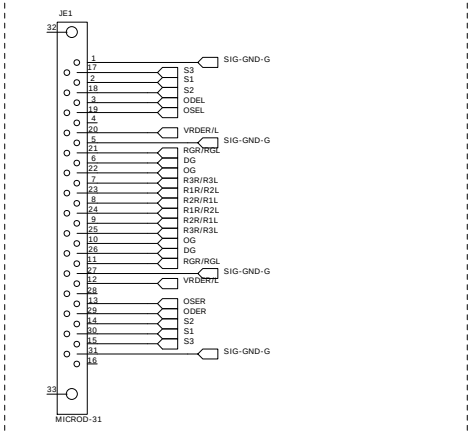
GUIDE SOUTH



GUIDE NORTH

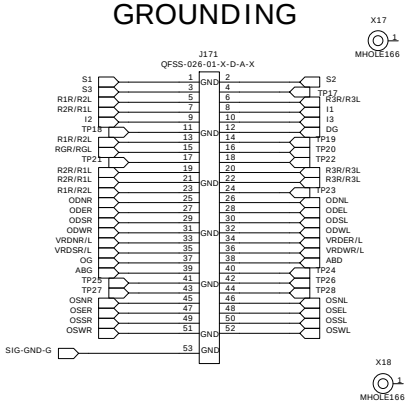


GUIDE EAST

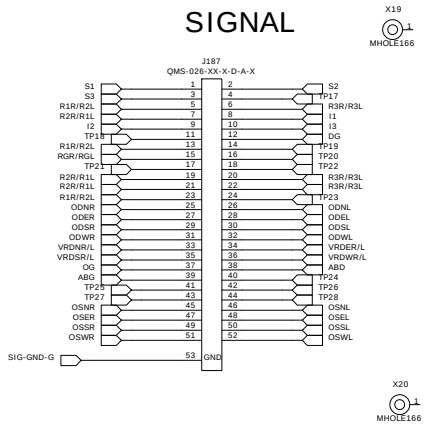


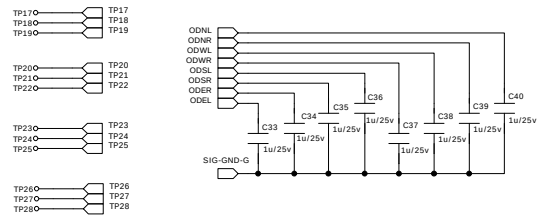
in vacuum

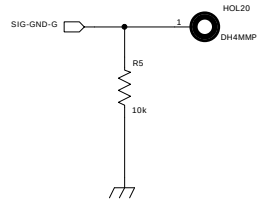
GROUNDING



SIGNAL







COMPANY: THE OHIO STATE UNIVERSITY DEPARTMENT OF ASTRONOMY IMAGING SCIENCES LABORATORY					
TITLE: GUIDE_CCDS					
DRAWN: moj	DATED: 9/30/2013	CODE:	SIZE: C	DRAWING NO: Wallboard.sch	REV: A
CHECKED:	DATED:	SCALE: NONE		SHEET: 3 OF 3	

Field Replacement of Wall Board

1. Shut down compressors < install shorting plugs Remove and STO Blue Cables
2. Wait for all temperatures to be above ~~Brooks minimum disconnect temperature~~ 10 C
3. Disconnect six CT lines at ~~cold heads~~ ELBOWS
4. Stow CT lines and elbows at top ring
5. Install jib-crane
6. Position telescope
7. Remove Dewar from top ring and place on projector cart
8. Move projector cart to clean tent http://www.ceramisis.com/inflatable_cleanroom.htm Model S 225 would be a candidate perhaps a 675.
9. Check that temperatures are above dew-point
10. Vent Dewar
11.
12. Remove rear cover
13. Unbolt cross strap from Center Cylinder (might require new pry-tool/puller torquer design)
14. Remove M10 threaded rod (to simplify lifting/lowering Cross strap from Dewar)
15. Install "M10 Safety Bar" into M10 hole to prevent Center Cylinder from shifting and hitting DMP
16. Disconnect PT 30 RTDs (2), charcoal RTD (1), DMP RTD/heater 2x6, CCD RTD (1)
17. Remove rear cylinder assembly (man lift) and place on lower shelf of projector cart
18. Remove WB top and bottom connector covers
19. Remove Inner Ring to front cylinder bolts (access is through holes in Wall Board)
20.
21. Prepare 3 WB jack assemblies
22. Place Round Bubble level on WB to monitor the lift and keep WB level
23. Mount 2 jacks (277mm long hex bar, with ¼" thick rubber spacers) to WB at the 2 corner ¼" holes in WB. (Use ¼-20 hex head to connect hex bars to jack)
24. Mount third jack (283mm long hex bar, no rubber spacers) under WB ¼" hole outside connector cover area. (Use ¼-20 hex head to connect hex bar to jack)
25. Raise all three jacks lifting WB + DMP assembly until Rear surface of DMP is at the level of the Front Cylinder to Wall Board O-Ring, about 4".
26. Remove ONLY one of the M5 SHCS from each of the DMP nut blocks where the lift support blocks will be installed (the second M5 SHCS retains the nut block in case the epoxy has failed).
27. Install three lift support blocks using the 4mm hex on a knob. Tighten with "L" allen wrench. Only one of the M5 captive SHCS is used so the support block is staggered relative to the nut block.
28. Lower assembly onto lift support blocks (jacks can remain in place or removed and set aside). Blocks rest on O-ring, do not damage O-ring.
29.
30. Check that all E-rings on shorting blocks are not distorted prior to installation of plugs.
31. Disconnect flex cables installing shorting plugs as you go

32. Remove four WB retaining shoulder bolts
33. Replace offending Wall Board
34. Tools required include 0.050" allen driver for Axon connectors and 1/16" allen driver for the Glenair shorting plugs. All three sites have a 1/8" nut driver and a 1/8" combination wrench to re-tighten jack posts on the flexis.

a. Verify that all 16 connectors are fully mated
b. Check that all E-rings on shorting plugs are still present after mating flexis
c. The tails on the micro-D connectors must be inspected and trimmed if too long. Re-check for shorts and bridges

35. Raise DMP assembly with jacks to relieve load on support blocks
36. Remove support blocks (4mm allen wrench and using the 4mm hex on a knob) then re-install second M5 SHCS into all three DMP nut blocks
37. Carefully lower DMP assembly into Dewar until Inner Ring mates with Front Cylinder
38. Install Inner Ring to front cylinder bolts
39. Remove all three jacks and hex bars from WB assembly
40. Install WB top and bottom connector covers with standoffs
41. Install rear cylinder assembly (man lift) onto Wall Board (check & clean inverted O-ring and groove)
42. Remove "M10 Safety Bar" from M10 hole
43. Install M10 threaded rod through hole in cross-strap (10 turns of engagement)
44. Re-bolt cross strap to Center Cylinder with large Belleville washer and M10 hex nut
45. Re-connect PT 30 RTDs (2), charcoal RTD (1), DMP RTD/heater 2x6, CCD RTD (1)
46. Re-install rear cover
47. Follow Procedure for Re-connecting blue cables
48. Re-install Camera on telescope
49. Re-connect cryocooler lines
50. Pump Dewar with vacuum pump
51. Start PT30 #1 compressor, then wait 20 seconds
52. Start PT30 #2 compressor
53. Wait for PT30 temperatures drop to -80C
54. Start PT13 compressor

				K-1		K-2	
				M-2		M-1	
				T-1		T-2	
				N-2		N-1	
Samtec pins					more		more
	d	Nominal V		J36	J36	J77	J77
1	8	clock	A1	1	26		
2	9	clock	A2	2	25		
3	10	clock	A3	51	27		
4	11	clock	A4	50	28		
5	0	clock	E1	40			
6	1	clock	E3	39			
7	2	clock	E2	38			
8	12	clock	D1			50	28
9	13	clock	D2			51	27
10	14	clock	D3			2	25
11	15	clock	D4			1	26
12	6	clock	TGA	3	24		
13	0	clock	E1				
14	4	clock	SWE	14			
15	5	clock	RGE	13			
16	hi	clock HI	rgd,swd,ogd,g1,g2,g3			13,14,37,38,39,40	
17	lo	clock LO	TGD			3,24	
18	7	clock	PREP (NC)				
19	1	clock	E2				
20	2	clock	E3				
21	1	clock	E2				
22	2	clock	E3				
23	0	clock	E1				
24	4>5	clock	DMY(NU)				
25		28	OD1	4			
26		28	OD2	6			
27		28	OD3	8			
28		28	OD4	10			
29		28	OD5	17			
30		28	OD6	19			
31		28	OD7	21			
32		28	OD8	23			
33		17	RD1/2	29			
34		17	RD3/4	33			
35		17	RD5/6	45			
36		17	RD7/8	49			
37		2	OG	37			
38		20	DDA/ddd	41		41	
39		17	od9-16			4,6,8,10,17,19,21,23	
40		17	rd9-16			29, 33, 45, 49	
41							
42							
43							
44							
45			OS 1	5			
46			OS 2	7			
47			OS 3	9			
48			OS 4	11			
49			OS 5	16			
50			OS 6	18			
51			OS.7	20			
53			ss	12,15,31,35,43,47		12,15,31,35,43,47	
			DOS1	30	open		
			DOS2	32	open		
			DOS3	34	open		
			DOS4	36	open		
			DOS5	42	open		
			DOS6	44	open		
			DOS7	46	open		
			DOS8	48	open		
			dos9		open	30	
			dos10		open	32	
			dos11		open	34	
			dos12		open	36	
			dos13		open	42	
			dos14		open	44	
			dos15		open	46	
			dos16		open	48	
			os9		open	5	
			os10		open	7	
			os11		open	9	
			os12		open	11	
			os13		open	16	
			os14		open	18	
			os15		open	20	
			os16		open	22	

goes to J168 PIN	Jumper to resistor pad and signal name	(TPs on adapter board) Mate for Proto Wall Broad J24	old pins CBB	new pins	d	Nominal V		K-1 M-2 T-1 N-2 J36	more J36	K-2 M-1 T-2 N-1 J77	more J77
		1	52	1	8	clock	A1	1	26		
		2	51	2	9	clock	A2	2	25		
		24	50	3	10	clock	A3	51	27		
		25	49	4	11	clock	A4	50	28		
		33	48	5	0	clock	E1	40			
		32	47	6	1	clock	E3	39			
		31	46	7	2	clock	E2	38			
		48	45	8	12	clock	D1			50	28
		47	44	9	13	clock	D2			51	27
		50	43	10	14	clock	D3			2	25
		49	42	11	15	clock	D4			1	26
		3,39	41	12	6	clock	TGA	3	24		
			40	13	0	clock	E1				
		14	39	14	4	clock	SWE	14			
		13	38	15	5	clock	RGE	13			
5	R26 (OS1-N)	TP16	37	16	hi	clock HI	rgd,swd,ogd/d ,g1,g2,g3			13,14,37,38,39,40	
7	R29 (OS2-N)	TP17	36	17	lo	clock LO	TGD		? OGP only	3,24	
9	R27 (OS3-N)	TP18	35	18	7	clock	PREP (NC)				
11	R28 (OS4-N)	TP19	34	19	1	clock	E2				
		TP20	33	20	2	clock	E3				
		TP21	32	21	1	clock	E2				
		TP22	31	22	2	clock	E3				
		TP23	30	23	0	clock	E1				
		TP24	29	24	4>5	clock	DMY(NU)				
		4	28	25		28	OD1	4			
		6	27	26		28	OD2	6			
		8	26	27		28	OD3	8			
		10	25	28		28	OD4	10			
		17	24	29		28	OD5	17			
		19	23	30		28	OD6	19			
		21	22	31		28	OD7	21			
		23	21	32		28	OD8	23			
		26	20	33		17	RD1/2	29			
		28	19	34		17	RD3/4	33			
		36	18	35		17	RD5/6	45			
		38	17	36		17	RD7/8	49			
		30	16	37		2	OG	37			
		34	15	38		20	DDA/ddd	41		41	
16	R30 (OS5-N)	TP39	14	39		17	od9-16			4,6,8,10,17,19,21,23	
18	R32 (OS6-N)	TP40	13	40		17	rd9-16			29, 33, 45, 49	
20	R31 (OS7-N)	TP41	12	41							
22	R33 (OS8-N)	TP42	11	42							
		TP43	10	43							
		TP44	9	44							
		5	8	45			OS 1	5			
		7	7	46			OS 2	7			
		9	6	47			OS 3	9			
		11	5	48			OS 4	11			
		16	4	49			OS 5	16			
		18	3	50			OS 6	18			
		20	2	51			OS.7	20			
		22	1	52			OS 8	22			
		37,40,41,42,43,44,45,46	53	53			ss	12,15,31,35,43,47		12,15,31,35,43,47	
							DOS1	30	open		
							DOS2	32	open		
							DOS3	34	open		
							DOS4	36	open		
							DOS5	42	open		
							DOS6	44	open		
							DOS7	46	open		
							DOS8	48	open		
							dos9		open	30	
							dos10		open	32	
							dos11		open	34	
							dos12		open	36	
							dos13		open	42	
							dos14		open	44	
							dos15		open	46	
							dos16		open	48	
	E1	Clocks 5,13,23					os9		open	5	
	E2	Clocks 7,19,21					os10		open	7	
	E3	Clocks 6,20,22					os11		open	9	
							os12		open	11	
							os13		open	16	
							os14		open	18	
							os15		open	20	
							os16		open	22	

1. The Detector Cables (5) are:

Samtec 6QCD-026-75.00-TRR-SBR-1-B

They are 52 coax cables with common ground, 75" long. One end with a male connector and the other with a female connector wired 1:1.

2. The cable for the Dewar RTDs is currently two detector cables connected in series (a single one is not long enough). It is planed to order 100" cables.

1. The Detector Cables (5) are:

Samtec 6QCD-026-75.00-TRR-SBR-1-B

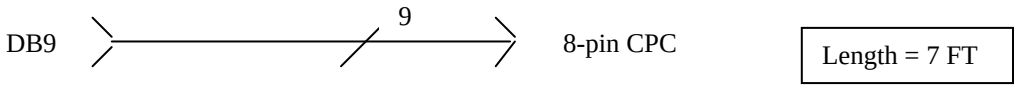
They are 52 coax cables with common ground, 75" long. One end with a male connector and the other with a female connector wired 1:1.

2. The cable for the Dewar RTDs is currently two detector cables connected in series (a single one is not long enough). It is planed to order 100" cables.
3. The DMP heat cable has a CPC on the HE end and a 9 pin D connector on the Wall Board end.
4. The Microion+ Cable has an RJ45 on the HE end and a 15 pin D connector on the gauge end.
5. The Shutter cable has a CPC on the HE end and a 37 pin D on the telescope end.
6. Ask Dan or Sang-Mok about the LED cable.

OSU
ISL

Wiring List

Instrument Name: KMT	Cable Desc.: Detector Mounting Plate (DMP) Heat Cable pinout
Component: Head Electronics	Component No.: N/A
Connector ID	Connector Desc.
1:	Tyco (Amp) 206434-1, 8-pin Series 2 CPC, cable male
2:	DB9 female
3:	
4:	
5:	



Wire ID#	Signal Name	Wire Type	Pair ID#	Wire Color	#1 pin	#2 pin	#3 pin	#4 pin	#5 pin
	RTD V+	DB9 26AWG			1	1			
	RTD V-	DB9 26AWG			2	7			
	RTD I+	DB9 26AWG			3	4			
	RTD I-	DB9 26AWG			4	2			
	Det Heat	DB9 26AWG			5	3			
	GND	DB9 26AWG			6	6			

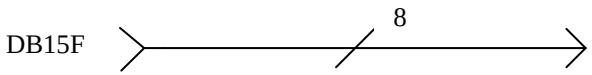
OSU
ISL

Wire ID#	Signal Name	Wire Type	Pair ID#	Wire Color	#1 pin	#2 pin	#3 pin	#4 pin	#5 pin

OSU
ISL

Wiring List

Instrument Name: KMT	Cable Desc.: Granville-Phillips Micro-Ion Plus RS485 pigtail
Component: Head Electronics	Component No.: N/A
Connector ID	Connector Desc.
1:	DB15F (15-pin female Game controller type)
2:	RJ45M (8-pin male plug ethernet type)
3:	
4:	
5:	



Length = 3 FT

Wire ID#	Signal Name	Wire Type	Pair ID#	Wire Color	#1 pin	#2 pin	#3 pin	#4 pin	#5 pin
	RS485+	Cat5 26AWG		Wh/Or	13	1			
	RS485-	Cat5 26AWG		Or	14	2			
	+24VDC	Cat5 26AWG		Wh/Gr, Wh/Bl	8	3, 5			
	GND	Cat5 26AWG		Bl, Gr	5	4, 6			

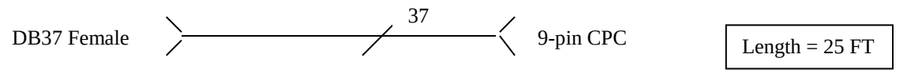
OSU
ISL

Wire ID#	Signal Name	Wire Type	Pair ID#	Wire Color	#1 pin	#2 pin	#3 pin	#4 pin	#5 pin

OSU
ISL

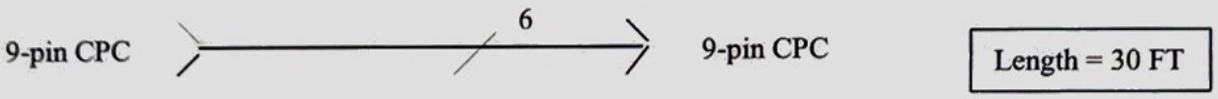
Wiring List

Instrument Name: KMT	Cable Desc.: Shutter Cable pinout
Component: Head Electronics	Component No.: N/A
Connector ID	Connector Desc.
1:	Tyco (Amp) 206485-1, 9-pin Series 2 CPC, cable female
2:	DB37 Female
3:	
4:	
5:	

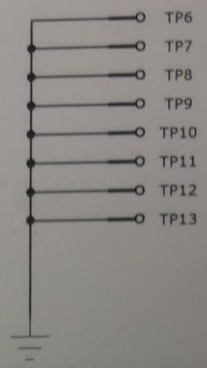


Wire ID#	Signal Name	Wire Type	Pair ID#	Wire Color	#1 pin	#2 pin	#3 pin	#4 pin	#5 pin
	Shutter Relay COM	DB37 26AWG			4	10			
	Shutter Relay NC	DB37 26AWG			5	11			

Instrument Name: KMT	Cable Desc.: LED Cable pinout
Component: Head Electronics	Component No.: N/A
Connector ID	Connector Desc.
1:	Tyco (Amp) 206485-1, 9-pin Series 2 CPC, cable female
2:	Tyco (Amp) 206486-1, 9-pin Series 2 CPC, panel male
3:	
4:	
5:	



Wire ID#	Signal Name	Wire Type	Pair ID#	Wire Color	#1 pin	#2 pin	#3 pin	#4 pin	#5 pin
	Preflash LED +	Telco 26AWG			1	1			
	GND LED -	Telco 26AWG			2	2			
	Not Used	Telco 26AWG			3	3			
	Not Used	Telco 26AWG			4	4			
	Not Used	Telco 26AWG			5	5			
	Not Used	Telco 26AWG			6	6			

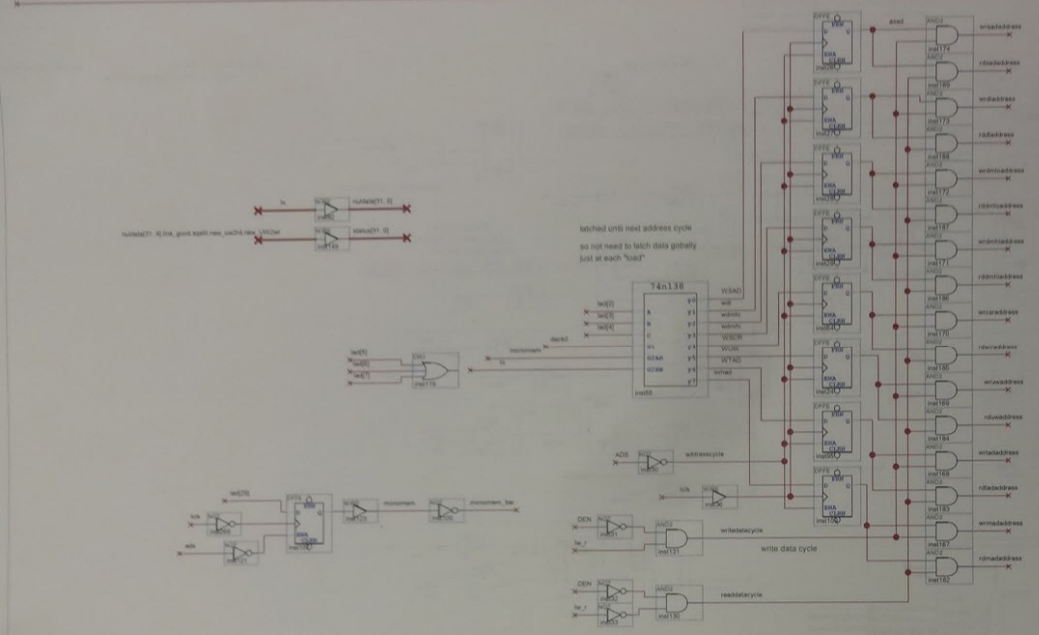


A

COMPANY: THE OHIO STATE UNIVERSITY DEPARTMENT OF ASTRONOMY IMAGING SCIENCES LABORATORY					
TITLE: PCI SQUENCER					
DRAWN: moj	DATED: March 2011	CODE:	SIZE: C	DRAWING NO: seq_reva.sch	REV: A
CHECKED:	DATED:	SCALE: NONE		SHEET: 1 OF 7	

KMTN 9K
Waveforms

Dewpoint
Sensor

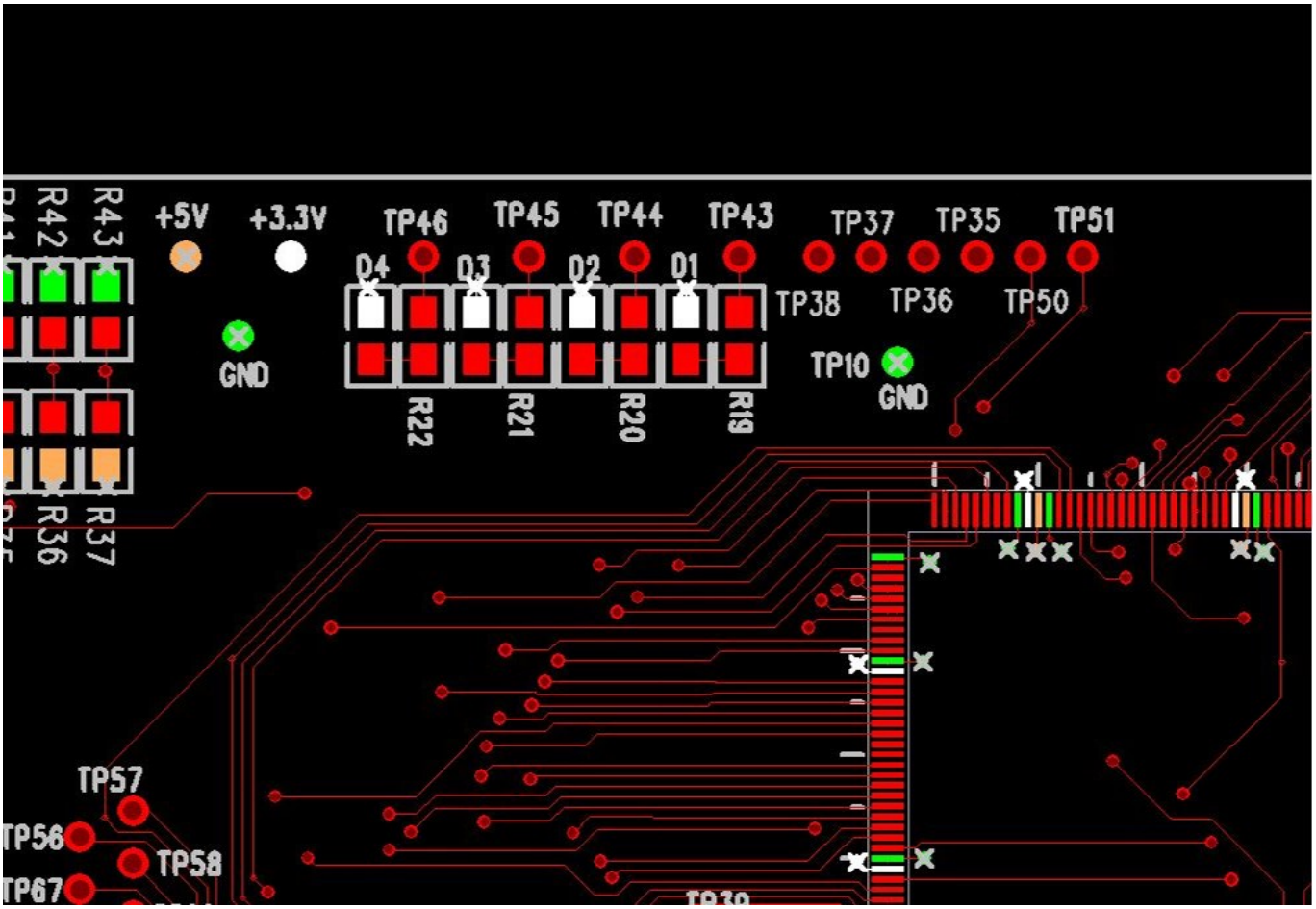


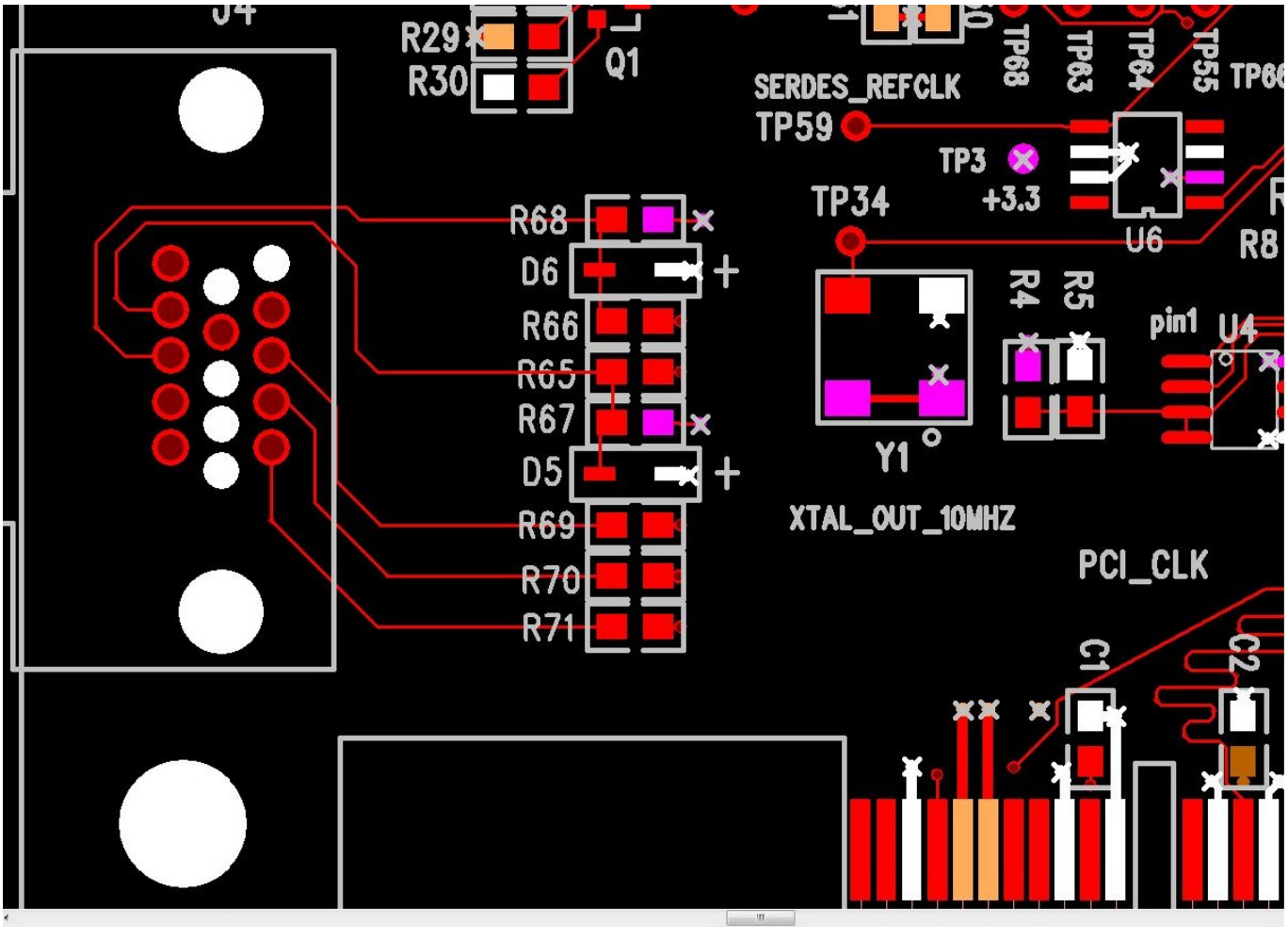
LFI_bar is low if link bad and vtiosc is selected when lifbar goes hi counter runs for 1ms. aeb goes

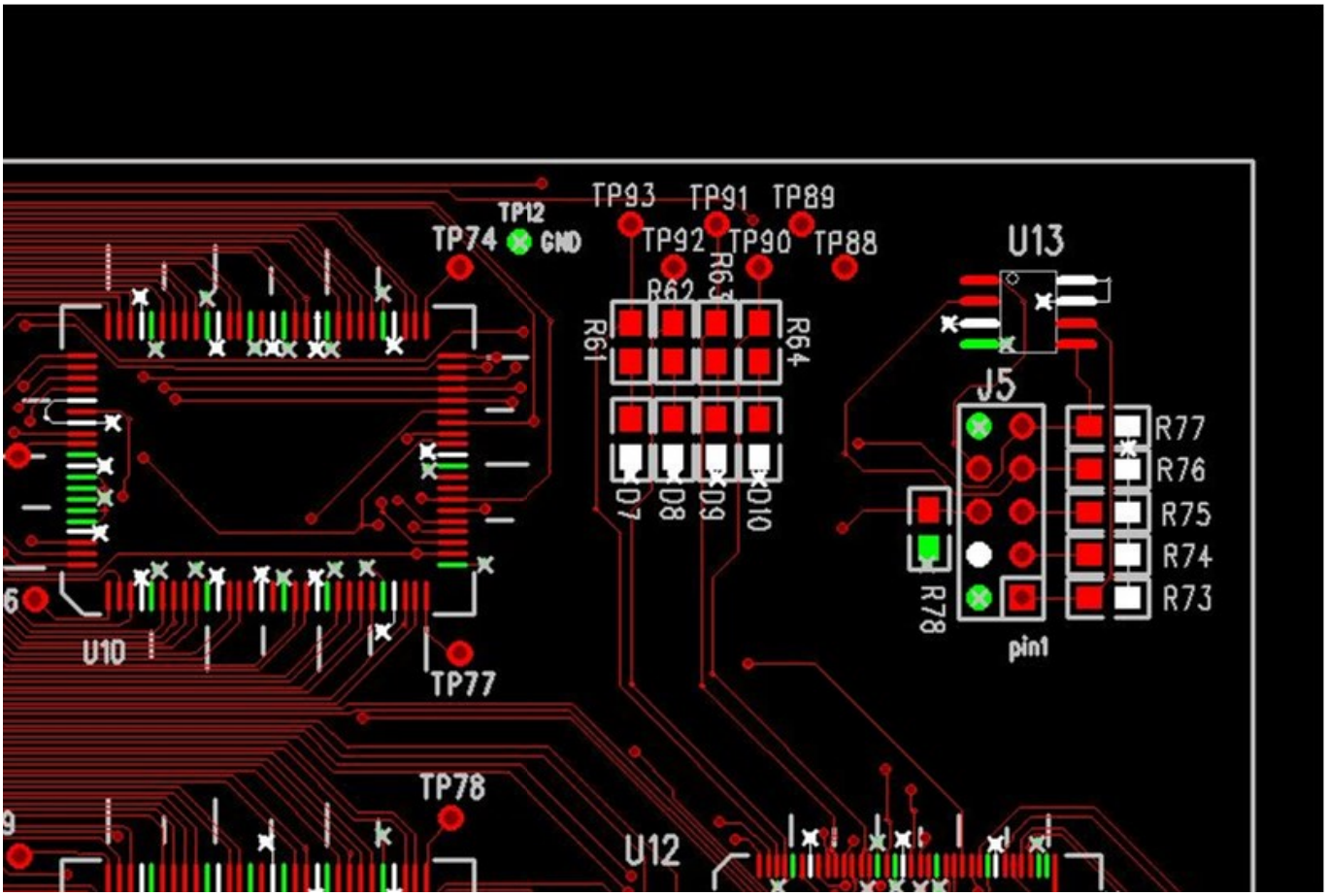
e2v Data Sheets
CCD 204 39 & CCD47-20

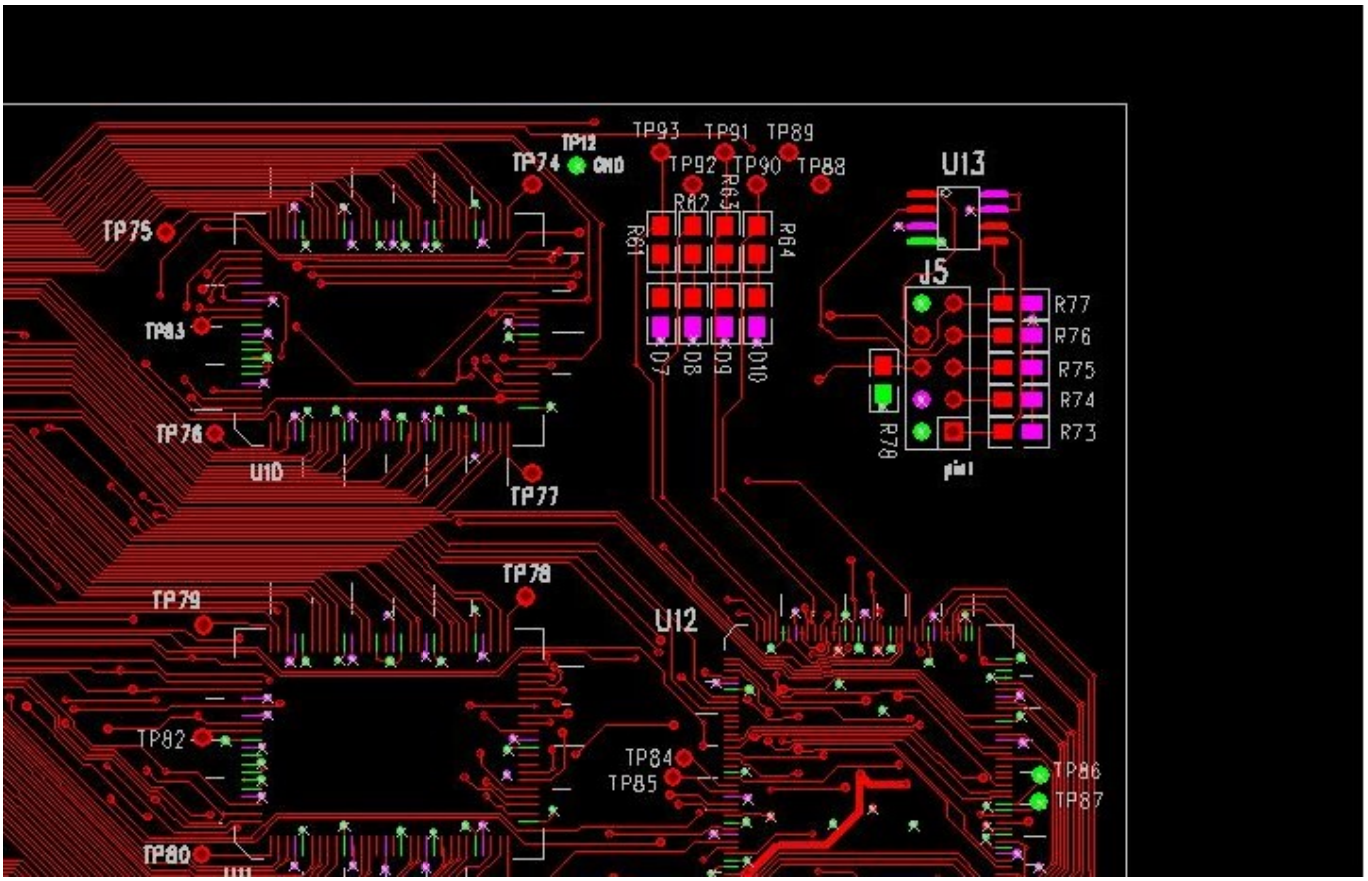
Waveforms Sensor

Item	Qty	Reference	Digi-Key part number	Description	Value	Price each
1	2	D5-6	1N4148WTPMSCT-ND	1N4148 diode	1N914	0.42
2	1	U4	93LC56B-I/SN-ND	EEPROM	93LC56B	0.34
3	2	J3 J5		10-pin JTAG header	NO LOAD	
4	4	C1-4	399-1166-1-ND	SURFACE MOUNT CAPACITOR 0805	0.047u	0.12
5	56	C7 C9 C13-14 C16-17 C19-20 C22-27 C29-30 C32-33 C35-37 C39-43 C45-46 C48-49 C51 C53-55 C57-59 C61-63 C65-69 C71-72 C75-76 C79-81 C83-86	399-1170-1-ND	SURFACE MOUNT CAPACITOR 0805	0.1u	0.0378
6	24	C5 C8 C11-12 C15 C18 C21 C28 C31 C34 C38 C44 C47 C50 C52 C56 C60 C64 C70 C73-74 C77-78 C82	445-3458-1-ND	SURFACE MOUNT CAPACITOR 0805	10u	0.154
7	2	C6 C10	490-1807-1-ND	SURFACE MOUNT CAPACITOR 0805	1u	0.366
8	1	J4	A35116-ND	VGA female connector PCB mount RA	VGA connector	1.96
9	2	U10-11	428-1629-ND	512K X 36 RAM	CY7C1380D-167AXC	32.08
10	1	U8	CY7C9689A-AXC-ND	TAXI Compatible Inteface	CY7C9689A-AXC	78.61
11	1	U12	544-1666-ND	Altera Cyclone II FPGA	EP2C8T	19.2
12	1	U7	544-1231-5-ND	Configuration Device DIP8 EPC1	NO LOAD	11
13	1	U13	544-1379-5-ND	IC CONFIG DEVICE 4MBIT 8-SOIC	EPCS4SI8N	13
14	1	U5	544-1280-ND	Altera Flex 6000	EPF6016	29.95
15	1	Q1	FDV303NCT-ND	N-Channel MOSFET	FDV303N	0.49
16	1	L3	445-6762-6-ND	Inductor 0805	10u	0.11
17	2	L1-2	445-3611-1-ND	Inductor 0805	1u	0.21
18	1	U2	497-6974-1-ND	1.2 V regulator D-Pak	LD1117S12CTR	0.54
19	1	U1	497-1236-1-ND	3.3 V regulator D-Pak	LD1117DT33TR	0.61
20	4	D2 D4 D8 D10	475-1406-1-ND	LED SMT	green	0.17
21	4	D1 D3 D7 D9	475-2510-1-ND	LED SMT	red	0.16
22	2	X1 X3		Mounting Hole	NO LOAD	
23	1	X2		Mounting Hole	NO LOAD	
24	1	U6	NB3N502DGOS-ND	Clock Multiplier PLL SOIC8	NB3N502DG	3.5
25	1	U3	Mouser 862-PCI9054-AC50PI-F	PCI Interface	PCI9054	76.65
26	1	J1		PCI Edge Connector Universal	NO LOAD	
27	7	R30 R39 R41 R43 R52-53 R79	RMCF0805ZT0R00CT-ND	SURFACE MOUNT RESISTOR 0805	0	0.03
28	1	R28	RMCF0805FT100KCT-ND	SURFACE MOUNT RESISTOR 0805	100k	0.04
29	2	R48-49	RHM102CCT-ND	SURFACE MOUNT RESISTOR 0805	102	0.041
30	33	R1-4 R6-14 R17-18 R32-37 R56-60 R72-78	RMCF1/1010KFRCT-ND	SURFACE MOUNT RESISTOR 0805	10k	0.029
31	1	R31	RHM11.3KCRCT-ND	SURFACE MOUNT RESISTOR 0805	11.3k	0.038
32	2	R65-66	RHM150KCT-ND	SURFACE MOUNT RESISTOR 0805	150	0.083
33	14	R19-27 R29 R61-64	311-1.00KCRCT-ND	SURFACE MOUNT RESISTOR 0805	1k	0.021
34	2	R54-55	RMCF0805JT200RCT-ND	SURFACE MOUNT RESISTOR 0805	200	0.03
35	3	R69-71	RHM270KCRCT-ND	SURFACE MOUNT RESISTOR 0805	270	0.042
36	4	R15-16 R67-68	RHM4.70KCRCT-ND	SURFACE MOUNT RESISTOR 0805	4k7	0.042
37	2	R50-51	RHM66.5CRCT-ND	SURFACE MOUNT RESISTOR 0805	66.5	0.038
38	2	R44-45	RMCF0805FT68R1CT-ND	SURFACE MOUNT RESISTOR 0805	68.1	0.04
39	2	R46-47	RMCF0805FT86R6CT-ND	SURFACE MOUNT RESISTOR 0805	86.6	0.04
40	5	R5 R38 R40 R42 R80		SURFACE MOUNT RESISTOR 0805	NO LOAD	
41	1	U9	A97430CT-ND, A97415-ND	SFP MODULE CONNECTOR W/ CAGE		2.70 + 6.03
42	93	TP1-93		0.033" test point	NO LOAD	
43	1	Y1	XC288CT-ND	Oscillator SMD	10 MHz	3.08


R43
R42
+5V
+3.3V
TP46
TP45
TP44
TP43
TP37
TP35
TP51
D4
D3
D2
D1
TP38
TP36
TP50
GND
TP10
GND
R22
R21
R20
R19
R37
R36
TP57
TP56
TP58
TP67


R29
R30
Q1
SERDES_REFCLK
TP59
TP68
TP63
TP64
TP55
TP3
+3.3
TP34
U6
R68
D6
R66
R65
R67
D5
R69
R70
R71
R4
R5
pin1
U4
Y1
XTAL_OUT_10MHZ
PCI_CLK
C1
C2


TP12
TP74
GND
TP93
TP91
TP89
TP92
TP90
TP88
U13
R62
R63
R61
R64
J5
D7
D8
D9
D10
R77
R76
R75
R74
R73
R78
pin1
U10
TP77
TP78
U12


TP12
TP74
GND
TP93
TP91
TP89
TP92
TP90
TP88
U13
TP75
R62
R63
R61
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TP83
D7
D8
D9
D10
R77
R76
R75
R74
R73
R78
pin1
TP76
U10
TP77
TP78
TP79
U12
TP82
TP84
TP85
TP86
TP87
TP80

CCD290-99 Back Illuminated Scientific CCD Sensor
9216 x 9232 Pixels, Sixteen Outputs
Non-inverted Mode Operation
Provisional data sheet

INTRODUCTION

The CCD290 extends e2v's family of scientific CCD sensors and has been designed to provide a large image area for demanding astronomical and scientific imaging applications. Back-illuminated spectral response combined with very low read-out noise give exceptional sensitivity.

DESCRIPTION

The sensor has an image area having 9216 × 9232 pixels with registers at both top and bottom each with eight outputs for short read-out times. The pixel size is 10 µm square. The image area has two separately connected sections to allow full-frame or split full-frame read-out modes. Depending on the mode, the read-out can be through 8 or 16 of the output circuits. A fixed-barrier dump drain is also provided to allow fast dumping of unwanted data.

The output amplifier is designed to give very low noise at read-out rates of up to 3 MHz. The low output impedance simplifies the interface with external electronics and the optional dummy outputs are provided to facilitate common mode rejection.

The package provides a compact footprint with guaranteed flatness at cryogenic temperatures. Connections are made at the top and bottom of the device via two flexi connectors that also provide a thermal break. The sides may be close butted if needed.

Specifications are tested and guaranteed at 173K (–100 °C).

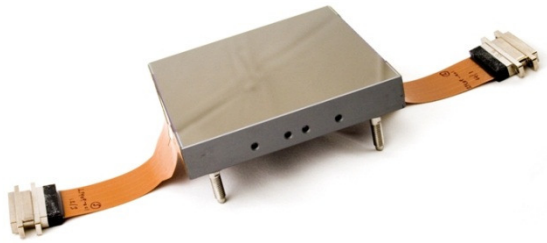
The CCD290 is a non-inverted (non-MPP) type.

VARIANTS

Standard silicon and deep-depletion silicon device types can be supplied with a range of AR coatings. Graded coatings and two-layer coatings are available as custom variants.

Devices with other formats (e.g. 4608 × 4608, or 6144 × 6144 pixels) or fewer outputs (4 or 8) may also be available to custom order.

Consult e2v technologies for further information on any of the above options.



[CCD231-C6 is illustrated here; CCD290-99 is similar]

SUMMARY PERFORMANCE (Typical)

Number of pixels	9216 (H) × 9232 (V)
Pixel size	10 µm square
Image area	92.2 mm × 92.4 mm
Outputs	16
Package size	98.5 × 93.7 mm
Package format	Silicon carbide with two flexi connectors
Focal plane height, above base	20.0 mm
Height tolerance	±15 µm
Connectors	Two 51-way micro-D
Flatness	<40 µm (peak to valley)
Amplifier sensitivity	7 µV/e^-
Read-out noise	4 e^- at 0.5 MHz 2.5 e^- at 50 kHz
Maximum pixel data rate	3 MHz
Charge storage (pixel full well)	90,000 e^-
Dark signal	2 e^-/pixel/hour (at –100 °C)

Quoted performance parameters given here are "typical" values. Specification limits are shown later.

Part References

CCD290-99-g-xxx

g = cosmetic grade
xxx = device-specific part number

CCD290-99-1-xxx	Grade-1, deep depletion, astro multi-2
CCD290-99-1-yyy	Grade-1, deep depletion, astro multi-7
CCD290-99-1-zzz	Grade-1, standard silicon, astro multi-2

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e2v technologies inc. 520 White Plains Road, Suite 450, Tarrytown, NY10591 USA Telephone: (914) 592-6050 Facsimile: (914) 592-5148 e-mail: enquiries@e2vtechnologies.us

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PERFORMANCE (At 173K unless stated)

Electro-Optical Specification (CCD290 Normal Mode, see note 1)

	Min	Typical	Max	Units	Note
Peak charge storage (image)	70,000	90,000	-	e^-/pixel	2(a)
Peak charge storage (register SW)	-	140,000	-	e^-/pixel	2(b)
Output node capacity: OG low (mode 1) OG high (mode 2)	 - -	 240,000 700,000	 - -	 e^- e^-	2(c)
Output amplifier responsivity: mode 1 mode 2	 5.0 -	 7.0 2.5	 - -	 µV/e^- µV/e^-	3
Read-out noise 50 kHz 500 kHz	 -	 2.5 4	 - 7	e^- rms	4
Maximum read-out frequency	-	1000	3000	kHz	5
Dark signal: at 173 K at 153 K	 - -	 2 0.02	 - 2.0	 e^-/pixel/hr e^-/pixel/hr	6
Charge transfer efficiency: parallel serial	 99.9990 99.9990	 99.9995 99.9995	 100 100	 % %	7
Spectral range	300	-	1060	nm	
Peak quantum efficiency	-	90	-	%	

NOTES

1. Device performance will be within the limits specified by “max” and “min” when operated at the recommended voltages supplied with the test data and when measured at a register clock frequency of approximately 0.1 – 1.0 MHz. Tests are performed at a nominal 500 kHz pixel rate.
2. (a) Signal level at which resolution begins to degrade. Device is non-inverted (NIMO/non-MPP), for maximum full well.

   (b) The summing well capacity limits the charge in the register. The limiting value may change in mode-2 but is not tested.

   (c) The signal handled by the output node (for linear operation) varies with mode as shown.
3. Under normal operation (mode 1), SW is operated as a summing well or clocked as RØ3. OG is biased at a low DC level.

   Alternatively (mode 2), SW may be operated as an output gate (and not therefore available for summing) and biased at a low DC level with OG raised to a high voltage (see note 9 later). This gives more charge-handling capacity (e.g. for higher level pixel binning). Charge transfer to the output now occurs as RØ2 goes low. In mode-2, the output noise will also increase by a factor of three. Mode-2 is not factory tested.
4. Noise is measured with correlated double sampling at 500 kHz nominal read-out rate (mode 1). The specification therefore applies at the 500 kHz measurement frequency. Performance at 50 kHz is also indicated (but not production-tested). If real and dummy outputs are used- differential noise is $\sqrt{2}$ higher.
5. The register will transfer charge at higher frequencies, depending on the external load capacitance to be driven, but performance cannot be guaranteed.
6. Dark signal is typically measured at a device temperature of 173 K. It is a strong function of temperature and the typical average (background) dark signal at any temperature T (Kelvin) between 150 K and 300 K is given by:

   $Q_d/Q_{do} = 122T^3e^{-6400/T}$

   where Q_{do} is the dark current at 293 K.

   Note that this is typical performance and some variation may be seen between devices.
7. Measured with a ^{55}Fe X-ray source. The CTE value is quoted for the complete clock cycle (i.e. not per phase).

SPECTRAL RESPONSE

The table below gives guaranteed minimum values of the spectral response for several variants. PRNU is also shown.

Standard silicon devices

	Standard silicon Astro Broadband	Standard silicon Astro Midband	Standard silicon Astro Multi-2	Maximum Pixel Response Non-Uniformity PRNU (1 σ) (%)
Wavelength (nm)	**Minimum QE (%)**	**Minimum QE (%)**	**Minimum QE (%)**	
350	40	20	30	-
400	70	50	75	3
500	80	80	75	-
650	75	80	80	3
900	25	25	25	5

Deep depletion devices

	Deep depletion silicon Astro Broadband	Deep depletion silicon Astro Midband	Deep depletion silicon Astro ER1 response	Deep depletion silicon Astro Multi-2	Deep depletion silicon Astro Multi-7	Maximum Pixel Response Non-Uniformity PRNU (1 σ) (%)
Wavelength (nm)	**Minimum QE (%)**	**Minimum QE (%)**	**Minimum QE (%)**	**Minimum QE (%)**	**Minimum QE (%)**	
350	40	20	20	30	-	-
400	70	50	35	75	45	3
500	75	80	65	75	75	-
650	70	80	80	80	80	3
900	40	40	45	50	50	5

Notes

The multi-AR coatings are currently considered as pre-production types prior to full process release.

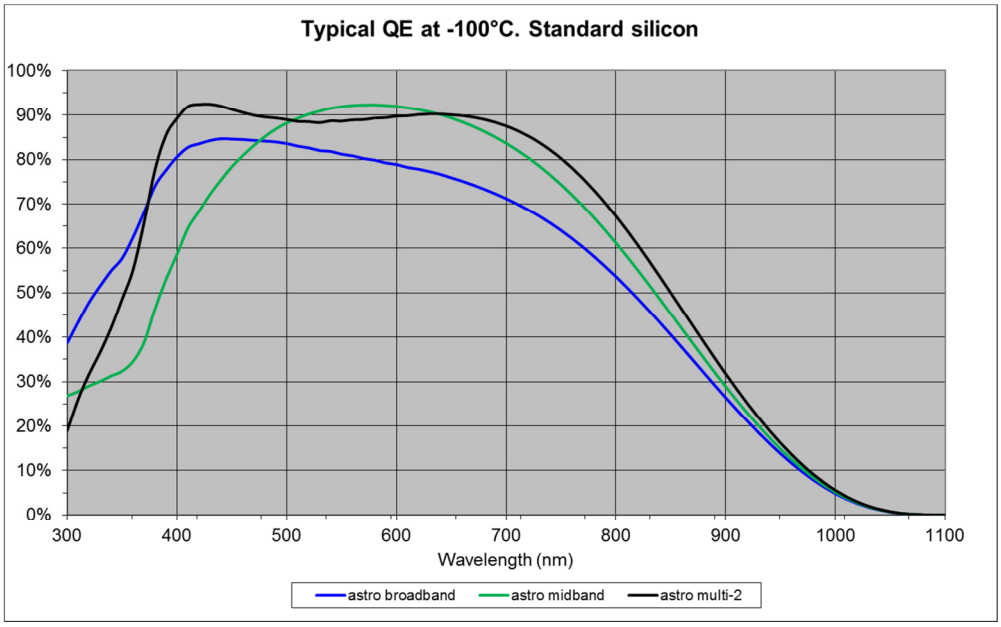
The multi-2 coating is designed for wide-range use.

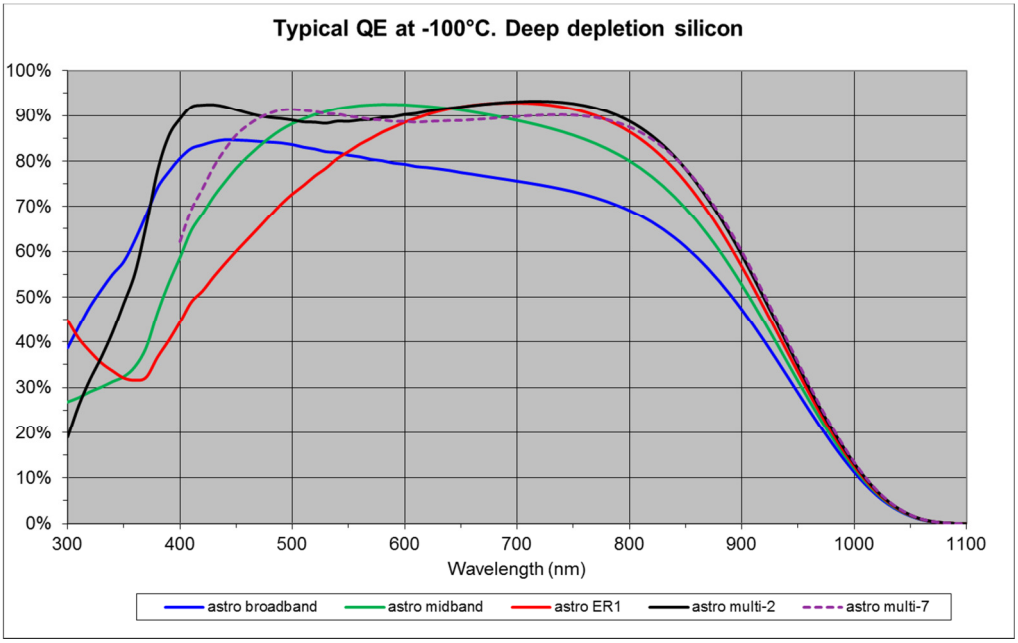
The multi-7 coating is designed specifically for the 500 to 1000 nm region; it has lower reflectivity (and fringing) than the multi-2 coating at the longest wavelengths.

Availability of coatings varies depending on type; check with factory.
Devices with an alternate spectral response may be available. Consult e2v technologies.

See also the figures below.

Typical Spectral response curves





COSMETIC SPECIFICATIONS

Maximum allowed defect levels are indicated below.

	Guaranteed Specifications			Typical Values		
Grade	**0**	**1**	**2**	**0**	**1**	**2**
Column defects - black or white	10	20	30	2	4	6
White spots	1000	2000	3000	<500	<1000	<1500
Total (black & white) spots	2000	4000	6000	<1000	<2000	<3000
Traps > 200e-	20	30	40	<10	<20	<30

Grade 1 is the default for general science use; consult the factory for grade-0 or grade-2availability.

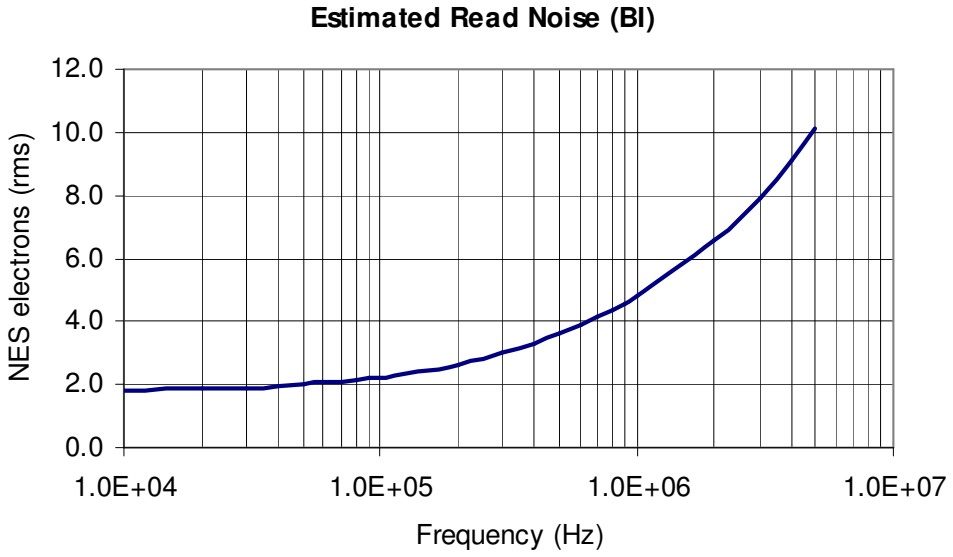
Grade 5 devices may also be available for set-up purposes. These are fully functional but with an image quality below that of grade 2, and may not meet all other specifications. Not all parameters may be tested.

DEFINITIONS

White spots	A defect is counted as a white spot if the dark generation rate is ≥ 5 e^-/pixel/s at 173 K. (which is also equivalent to ≥100 e^-/hour at 153 K). The temperature dependence is the same as for the mean dark signal; see note 6 above.
Black spots	A black spot defect is a pixel with a photo-response less than 50% of the local mean.
Column defects	A column is counted as a defect if it contains at least 100 white or dark single pixel defects.
Traps	A trap causes charge to be temporarily held in a pixel and these are counted as defects if the quantity of trapped charge is greater than 200 e^-
Defect exclusion zone	Defect measurements are excluded from the outer two rows and columns of the sensor.

AMPLIFIER READ NOISE

The variation of typical read noise with operating frequency is shown below. This is measured using correlated double sampling with a pre-sampling bandwidth equal to twice the pixel rate in mode 1, temperature range 150 – 230 K.



DEFINITIONS

Back-Thinning

A back-thinned CCD is fabricated on the front surface of the silicon and is subsequently processed for illumination from the reverse side. This avoids loss of transmission in the electrode layer (which can be particularly significant at shorter wavelengths or with low energy X-rays). This process requires the silicon to be reduced to a thin layer by a combination of chemical and mechanical means. The surface is “passivated” and an anti-reflection coating may be added.

AR Coating

Anti-reflection coatings are normally applied to the back illuminated CCD to further improve the quantum efficiency. Standard coatings optimise the response in the visible, ultra-violet or infrared regions. For X-ray detection an uncoated device may be preferable.

Read-out Noise

Read-out noise is the random noise from the CCD output stage in the absence of signal. This noise introduces a random fluctuation in the output voltage that is superimposed on the detected signal.

The method of measurement involves reverse-clocking the register and determining the standard deviation of the output fluctuations, and then converting the result to an equivalent number of electrons using the known amplifier responsivity.

Dummy Output

Each output has an associated “dummy” circuit on-chip, which is of identical design to the “real” circuit but receives no signal charge. The dummy output should have the same levels of clock feed-through, and can thus be used to suppress the similar component in the “real” signal output by means of a differential pre-amplifier. The penalty is that the noise is increased by a factor of $\sqrt{2}$. If not required the dummy outputs may be powered down.

Dark Signal

This is the output signal of the device with zero illumination. This typically consists of thermally generated electrons within the semiconductor material, which are accumulated during signal integration. Dark signal is a strong function of temperature as described in note 6.

Correlated Double Sampling

A technique for reducing the noise associated with the charge detection process by subtracting a first output sample taken just after reset from a second sample taken with charge present.

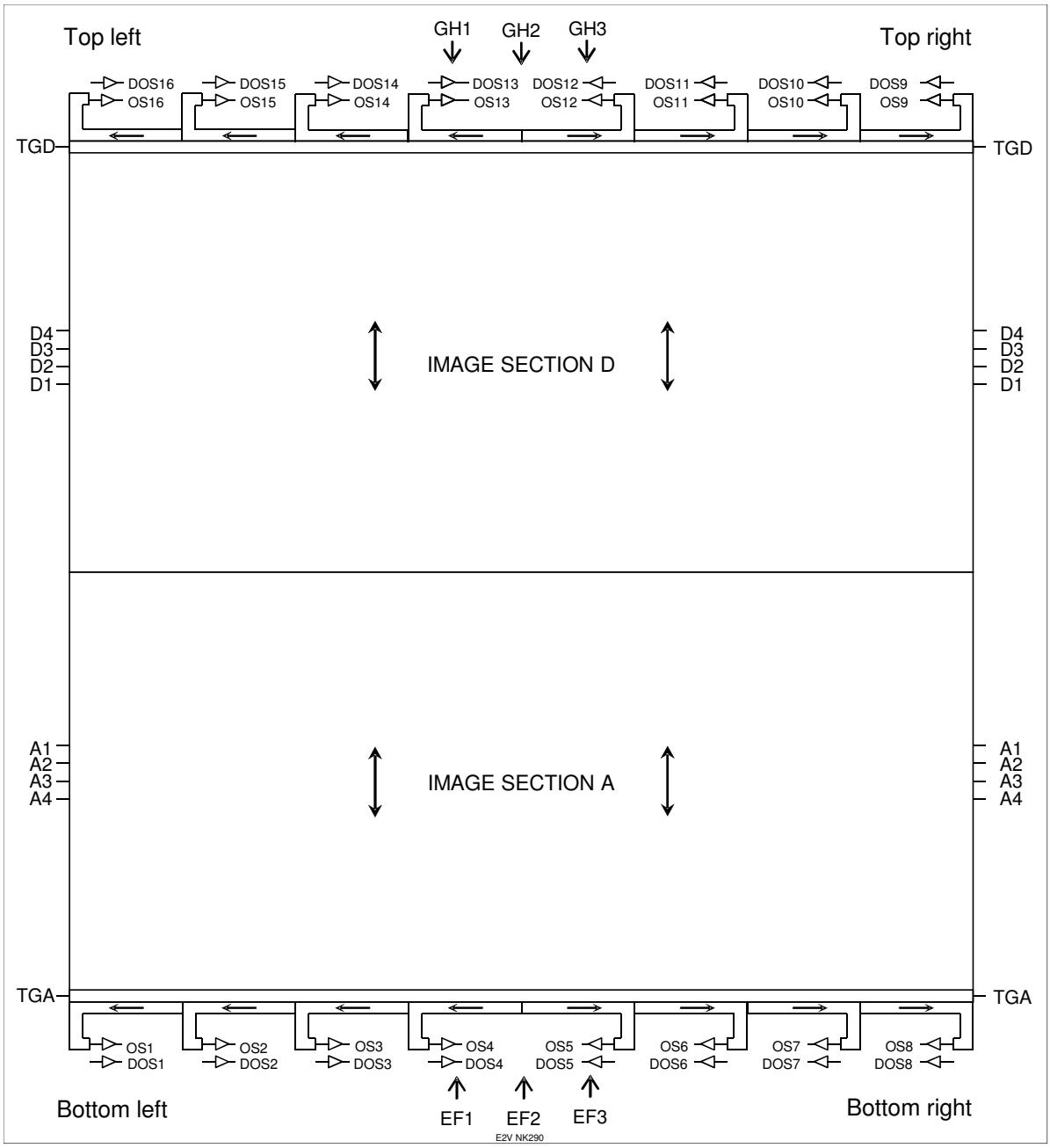
Charge Transfer Efficiency

The fraction of charge stored in a CCD element that is transferred to the adjacent element by a single clock cycle. The charge not transferred remains in the original element, possibly in trapping states and may possibly be released into later elements. The value of CTE is not constant but varies with signal size, temperature and clock frequency.

ARCHITECTURE

Chip Schematic

TOP



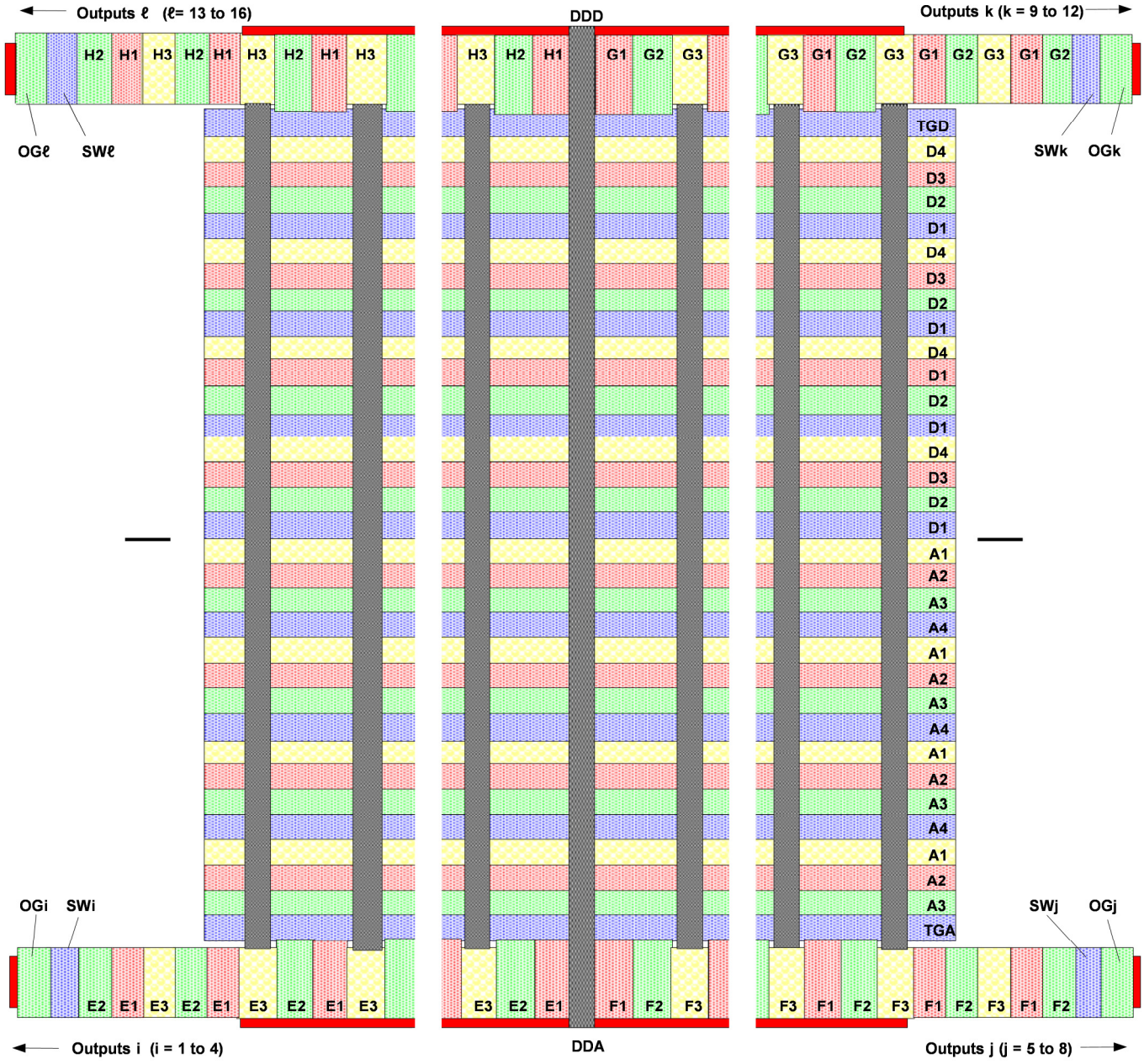
BOTTOM

Image sections A and D each have a total of 9216 (H) × 4616 (V) pixels.

Each register section has a total of 1179 elements: 1152 active and 27 pre-scan.

Connector-1 (and flexi) is at the “bottom” of the device (register EF); Connector-2 is at the “top” of the device (register GH).

ARRANGEMENT OF ELECTRODES

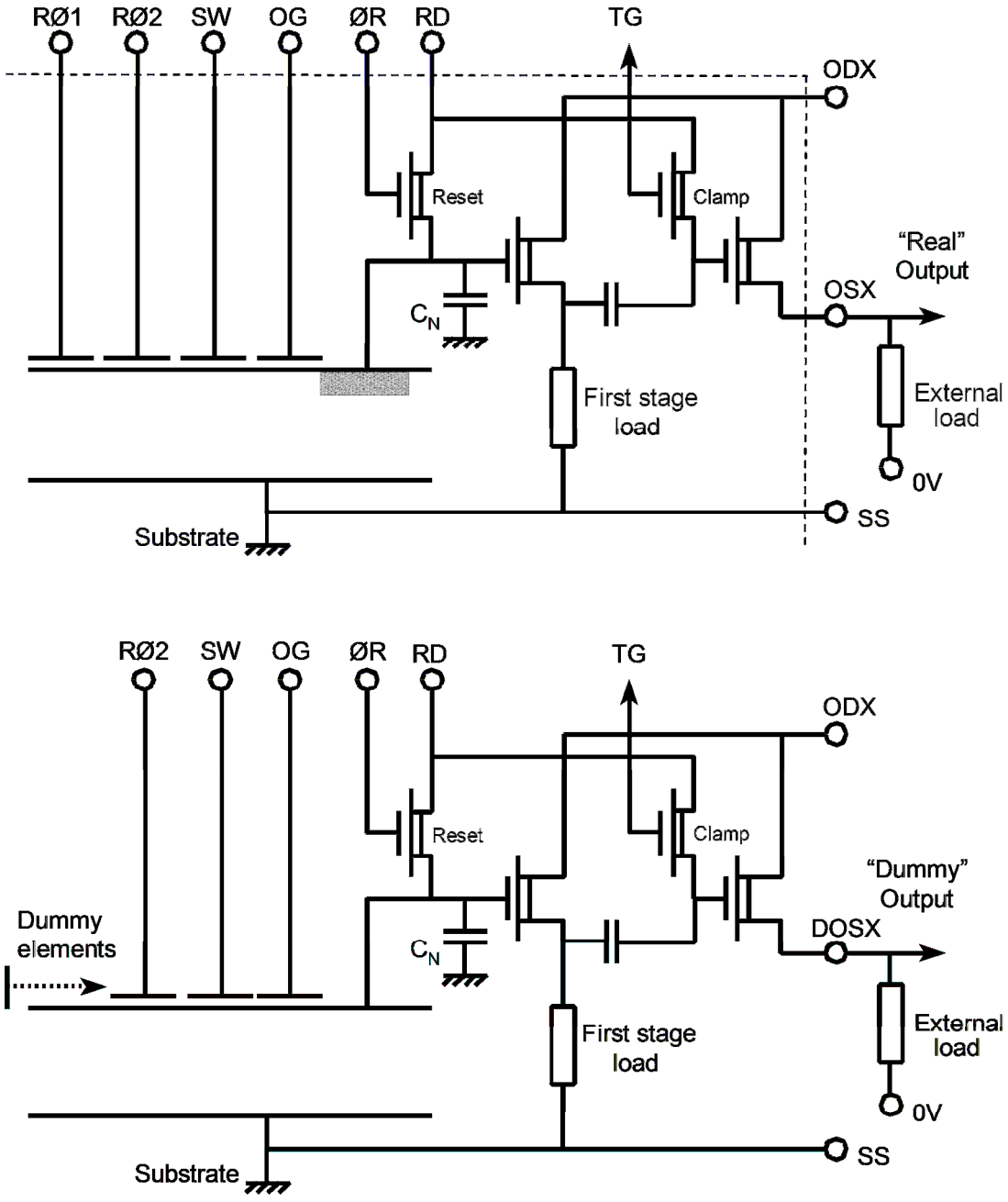


Pre-scan (blank) serial elements are not shown here.

Each output consists of real (OS) and dummy (DOS); see next page.

OUTPUT CIRCUIT

X designates a specific output, namely 1 to 16 (see the chip schematic).



The first stage load of each output (real or dummy) draws a quiescent current of approximately 0.2 mA via SS.

The output circuit consists of two capacitor-coupled source-follower stages. The particular design has a very high responsivity to give lowest noise. The load for the first stage is on-chip and that for the second stage is external, as next described. The DC restoration circuitry requires a pulse at the start of line readout, and this is automatically obtained by an internal connection to the adjacent transfer gate, TG. Transferring a line of charges to the register thus automatically activates the circuitry. N.B. TG pulses still need to be applied at similar intervals if only the register and/or output circuit are being operated, e.g. for test or characterisation purposes.

ELECTRICAL INTERFACES

CONNECTOR 1

PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (See note 10)			MAX RATINGS (V) with respect to V_{SS}
			Min	Typical	Max	
1	A1	Image Area A Clock Phase 1	9	10	12	±20
2	A2	Image Area A Clock Phase 2	9	10	12	±20
3	TGA	Image Area A Transfer gate	9	10	12	±20
4	OD1	Output Drain 1	25	28	31	-0.3 to +35
5	OS1	Output Source 1		(see note 8)		
6	OD2	Output Drain 2	25	28	31	-0.3 to +35
7	OS2	Output Source 2		(see note 8)		
8	OD3	Output Drain 3	25	28	31	-0.3 to +35
9	OS3	Output Source 3		(see note 8)		
10	OD4	Output Drain 4	25	28	31	-0.3 to +35
11	OS4	Output Source 4		(see note 8)		
12	SS	Substrate (see note 11)	0	0	10	N/A
13	ØRA	Reset Gate (A) (See note 12)	9	12	13	±20
14	SWA	Summing Well (A) (See note 9)	9	10	12	±20
15	SS	Substrate (see note 11)	0	0	10	N/A
16	OS5	Output Source 5		(see note 8)		
17	OD5	Output Drain 5	25	28	31	-0.3 to +35
18	OS6	Output Source 6		(see note 8)		
19	OD6	Output Drain 6	25	28	31	-0.3 to +35
20	OS7	Output Source 7		(see note 8)		
21	OD7	Output Drain 7	25	28	31	-0.3 to +35
22	OS8	Output Source 8		(see note 8)		
23	OD8	Output Drain 8	25	28	31	-0.3 to +35
24	TGA	Image Area A Transfer Gate	9	10	12	±20
25	A2	Image Area A Clock Phase 2	9	10	12	±20
26	A1	Image Area A Clock Phase 1	9	10	12	±20
27	A3	Image Area A Clock Phase 3	9	10	12	±20
28	A4	Image Area A Clock Phase 4	9	10	12	±20
29	RD1/2	Reset Drain (1/2)	16	17	19	-0.3 to +25
30	DOS1	Dummy Output Source 1		(see note 8)		
31	SS	Substrate (see note 11)	0	0	10	N/A
32	DOS2	Dummy Output Source 2		(see note 8)		
33	RD 3/4	Reset Drain (3/4)	16	17	19	-0.3 to +25
34	DOS3	Dummy Output Source 3		(see note 8)		
35	SS	Substrate (see note 11)	0	0	10	N/A
36	DOS4	Dummy Output Source 4		(see note 8)		
37	OGA	Output Gate (A) (See note 9)	1	2	(note 9)	±20
38	E3/F3	Register E & Register F Clock Phase 3	9	10	12	±20
39	E2/F2	Register E & Register F Clock Phase 2	9	10	12	±20
40	E1/F1	Register E & Register F Clock Phase 1	9	10	12	±20
41	DDA	Dump Drain (A) (See note 13)	15	18	20	-0.3 to +35
42	DOS5	Dummy Output Source 5		(see note 8)		
43	SS	Substrate (see note 11)	0	0	10	N/A
44	DOS6	Dummy Output Source 6		(see note 8)		
45	RD5/6	Reset Drain (5/6)	16	17	19	-0.3 to +25
46	DOS7	Dummy Output Source 7		(see note 8)		
47	SS	Substrate (see note 11)	0	0	10	N/A
48	DOS8	Dummy Output Source 8		(see note 8)		
49	RD7/8	Reset Drain (7/8)	16	17	19	-0.3 to +25
50	A4	Image Area A Clock Phase 4	9	10	12	±20
51	A3	Image Area A Clock Phase 3	9	10	12	±20

CONNECTOR 2

PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (See note 10)			MAX RATINGS (V) with respect to V_{SS}
			Min	Typical	Max	
1	D4	Image Area D Clock Phase 4	9	10	12	±20
2	D3	Image Area D Clock Phase 3	9	10	12	±20
3	TGD	Image Area D Transfer gate	9	10	12	±20
4	OD9	Output Drain 9	25	28	31	-0.3 to +35
5	OS9	Output Source 9		(see note 8)		
6	OD10	Output Drain 10	25	28	31	-0.3 to +35
7	OS10	Output Source 10		(see note 8)		
8	OD11	Output Drain 11	25	28	31	-0.3 to +35
9	OS11	Output Source 11		(see note 8)		
10	OD12	Output Drain 12	25	28	31	-0.3 to +35
11	OS12	Output Source 12		(see note 8)		
12	SS	Substrate (see note 11)	0	0	10	N/A
13	ØRD	Reset Gate (D) (See note 12)	9	12	13	±20
14	SWD	Summing Well (D) (See note 9)	9	10	12	±20
15	SS	Substrate (see note 11)	0	0	10	N/A
16	OS13	Output Source 13		(see note 8)		
17	OD13	Output Drain 13	25	28	31	-0.3 to +35
18	OS14	Output Source 14		(see note 8)		
19	OD14	Output Drain 14	25	28	31	-0.3 to +35
20	OS15	Output Source 15		(see note 8)		
21	OD15	Output Drain 15	25	28	31	-0.3 to +35
22	OS16	Output Source 16		(see note 8)		
23	OD16	Output Drain 16	25	28	31	-0.3 to +35
24	TGD	Image Area D Transfer Gate	9	10	12	±20
25	D3	Image Area D Clock Phase 3	9	10	12	±20
26	D4	Image Area D Clock Phase 4	9	10	12	±20
27	D2	Image Area D Clock Phase 2	9	10	12	±20
28	D1	Image Area D Clock Phase 1	9	10	12	±20
29	RD9/10	Reset Drain (9/10)	16	17	19	-0.3 to +25
30	DOS9	Dummy Output Source 9		(see note 8)		
31	SS	Substrate (see note 11)	0	0	10	N/A
32	DOS10	Dummy Output Source 10		(see note 8)		
33	RD11/12	Reset Drain (11/12)	16	17	19	-0.3 to +25
34	DOS11	Dummy Output Source 11		(see note 8)		
35	SS	Substrate (see note 11)	0	0	10	N/A
36	DOS12	Dummy Output Source 12		(see note 8)		
37	OGD	Output Gate (D) (See note 9)	1	2	(note 9)	±20
38	G3/H3	Register G & Register H Clock Phase 3	9	10	12	±20
39	G1/H1	Register G & Register H Clock Phase 1	9	10	12	±20
40	G2/H2	Register G & Register H Clock Phase 2	9	10	12	±20
41	DDD	Dump Drain (D) (See note 13)	15	18	20	-0.3 to +35
42	DOS13	Dummy Output Source 13		(see note 8)		
43	SS	Substrate (see note 11)	0	0	10	N/A
44	DOS14	Dummy Output Source 14		(see note 8)		
45	RD13/14	Reset Drain (13/14)	16	17	19	-0.3 to +25
46	DOS15	Dummy Output Source 15		(see note 8)		
47	SS	Substrate (see note 11)	0	0	10	N/A
48	DOS16	Dummy Output Source 16		(see note 8)		
49	RD15/16	Reset Drain (15/16)	16	17	19	-0.3 to +25
50	D1	Image Area D Clock Phase 1	9	10	12	±20
51	D2	Image Area D Clock Phase 2	9	10	12	±20

NOTES

8. Do not connect to voltage supply but use a ~5 mA current source or a ~5 kΩ external load. The quiescent voltage on OS is then about 6 - 8 V above the reset drain voltage and is typically 24 V. The current through these pins must not exceed 20 mA. Permanent damage may result if, in operation, OS or DOS experience short circuit conditions.

   For highest speed operation the output load resistor can be reduced from 5 kΩ to approximately 2.2 kΩ, but note that this will increase power consumption. If the device is to be operated with a register clock period of below about 1 MHz then the load may be increased to 10 kΩ to reduce power consumption.

9. Default operation (mode 1) shown with OG set to OG-Low, with a +2 V nominal value. In this mode SW may be clocked as RØ3 if a summing well function is not required. OG-Low should have a maximum value of +5 V.

   For alternative operation in a low responsivity mode (mode 2) with increased charge handling, OG should be set to OG-High and SW should be operated as OG-Low (i.e. 2V typical). See below for appropriate OG-High values. Charge is now read out as RØ2 goes low.

   See note 11 also for discussion about Substrate voltage (Vss). With high substrate voltage OG-High may be set to a nominal +20 V, which offers best linearity in mode-2. With low substrate voltage, the allowed maximum value of OG-High is limited to a nominal +18 V; the lower OG-High value has a greater non-linearity.

10. To ensure that any device can be operated the camera should be designed so that any value in the range “min” to “max” can be provided. All operating voltages are with respect to image clock low (nominally 0 V).

    The clock pulse low levels should be in the range 0 ± 0.5 V for image clocks. The register and SW clock low level should be +1 V higher. Reset clock low may be nominally 0 V or +1 V.

    In all cases, specific recommended settings will be supplied with each science-grade sensor.

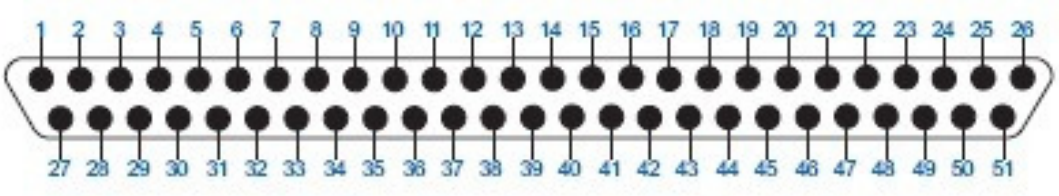
11. The substrate voltage (Vss) has a default value of 0 V (“low” substrate). This is particularly recommended for deep-depletion device variants, since it optimises depletion depth for best Point Spread Function. Devices may alternatively be operated at “high” substrate, with Vss = 9 V. The high substrate setting offers slightly lower dark current, although this is usually not of primary concern when the device is cryogenically cooled.

    The substrate setting has some consequence for the allowed OG upper voltage level, as discussed in note 9.

12. Standard silicon variants are expected to be used with ØR at +10 V or more; deep depletion variants require at least +12 V. A higher value will give a correspondingly higher reset feed-through signal in the device output (OS).

13. The DD function may change in future versions. Consult factory for information.
    The DD voltage level determines the level at which register overspill into the drain occurs.

PIN CONNECTIONS (View facing pins of connector)



This numbering applies to both connectors. The connector is a Glenair 51P micro D type.

ELECTRICAL INTERFACE CHARACTERISTICS

Electrode capacitances (defined at mid-clock level)

	Typical	Units
IØ/IØ inter-phase [A, D]	70	nF
IØ/SS per phase [A, D]	20	nF
Total IØ per phase (to Vss and two inter-phase)	160	nF
Transfer gates [TGA, TGD]	150	pF
RØ total per phase [each of E1/F1, G1/H1]	450	pF
RØ total per phase [each of E2/F2, G2/H2]	600	pF
RØ total per phase [each of E3/F3, G3/H3]	650	pF

The total capacitance to be driven per phase is the sum of the component to substrate and the inter-phase components to each of the adjacent phases.

The amplifier output impedance is typically 400 Ω.

POWER UP/POWER DOWN

When powering the device up or down it is critical that any specified maximum rating is not exceeded. Specifically the voltages for the amplifier and dump drains (OD, RD, DD) must never be taken negative with respect to the substrate. Hence, if the substrate is to be operated at a positive voltage (e.g. to minimise dark current) then the drive electronics should have a switch-on sequence which powers up all the drains to their positive voltages before the substrate voltage starts to increase from zero.

It is also important to ensure that excess currents (see note 8) do not flow in the OS or DOS pins. Such currents could arise from rapid charging of a signal coupling capacitor or from an incorrectly biased DC-coupled preamplifier.

Similarly, for powering down, the substrate must be taken to zero voltage before the drains.

POWER CONSUMPTION

The power dissipated within the CCD is a combination of the static dissipation of the amplifiers and the dynamic dissipation from the parallel and serial clocking (i.e. driving the capacitive loads).

The table below gives representative values for the components of the on-chip power dissipation for the case of continuous split-frame line-by-line readout using both registers and all the output circuits with both real and dummy amplifiers activated. The frequency is that for clocking the serial register and an appropriate value of the amplifier load is utilised in each case.

Read-out frequency	Line time	Amplifier load	Power dissipation			
			Amplifiers	Serial clocks	Parallel clocks	Total (approx)
1 MHz	1.5 ms	5 kΩ	800 mW	≤ 100 mW	≤ 100 mW	1 W

The dissipation reduces to only that of the amplifiers during the time that charge is being collected in the image sections with both the parallel and serial clocks static.

Each flex-cable has a thermal conductivity of approximately 1 mW/°C.

FRAME READ-OUT MODES

The device can be operated in a full-frame or split full-frame mode.

If the applied drive pulses are designated IØ1, IØ2, IØ3 and IØ4, then connections should be made as tabulated below to effect the following directions of transfer.

Clock Generator Drive Pulse Name	IØ1	IØ2	IØ3	IØ4	
A section transfer towards E register	A1	A2	A3	A4	TGA = IØ4
D section transfer towards G register	D1	D2	D3	D4	TGD = IØ1
A section transfer towards G register	A4	A3	A2	A1	TGA = “low”
D section transfer towards E register	D4	D3	D2	D1	TGD = “low”

The first two transfer sequences are for split frame read-out. The second two are for reversing the transfer direction in either section for read-out to either the top or the bottom register sections.

Transfer from the image section to the register is into the phase 1 and 2 electrodes, i.e. E/F1, G/H1, E/F2 and G/H2. These electrodes must be held at clock “high” level during the process. If the register pulses are designated RØ1, RØ2 and RØ3, then connections should be made as tabulated below.

Clock Generator Drive Pulse Name	RØ1	RØ2	RØ3
E section	E1/F1	E2/F2	E3/F3
G section	G1/H1	G2/H2	G3/H3

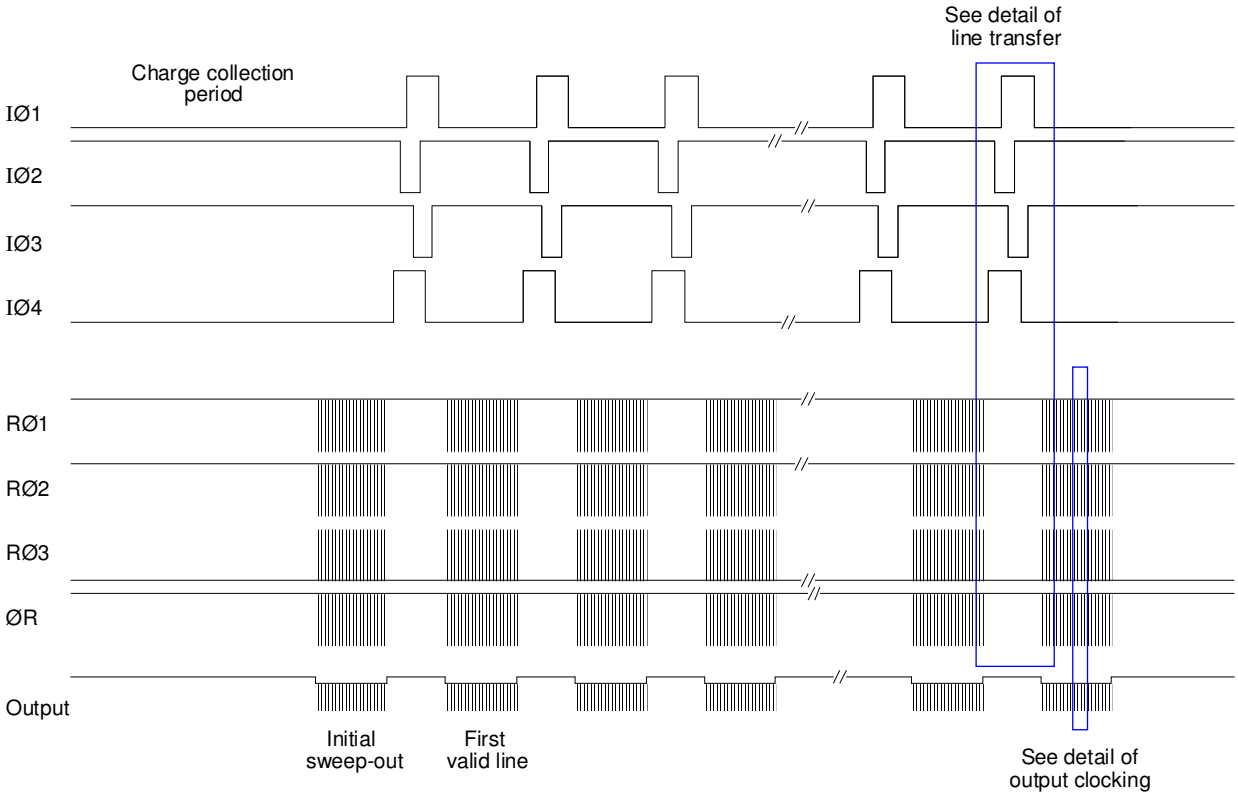
The last electrode before the output gate is separately connected to give the function of a summing well (SW). In normal readout (i.e. if not used for summing), SW is clocked as RØ3. For summing, the selected SW gate is held at clock “high” level for the required number of readout cycles, and then clocked as RØ3 to output charge.

Alternatively, SW may be operated as a second output gate to provide the option of operation in low gain/high signal mode (mode 2) with OG high. If this mode of operation is used, then the sequencing of the output clocks must be changed, as charge now transfers into the output node as RØ2 goes low (see note 9 above also).

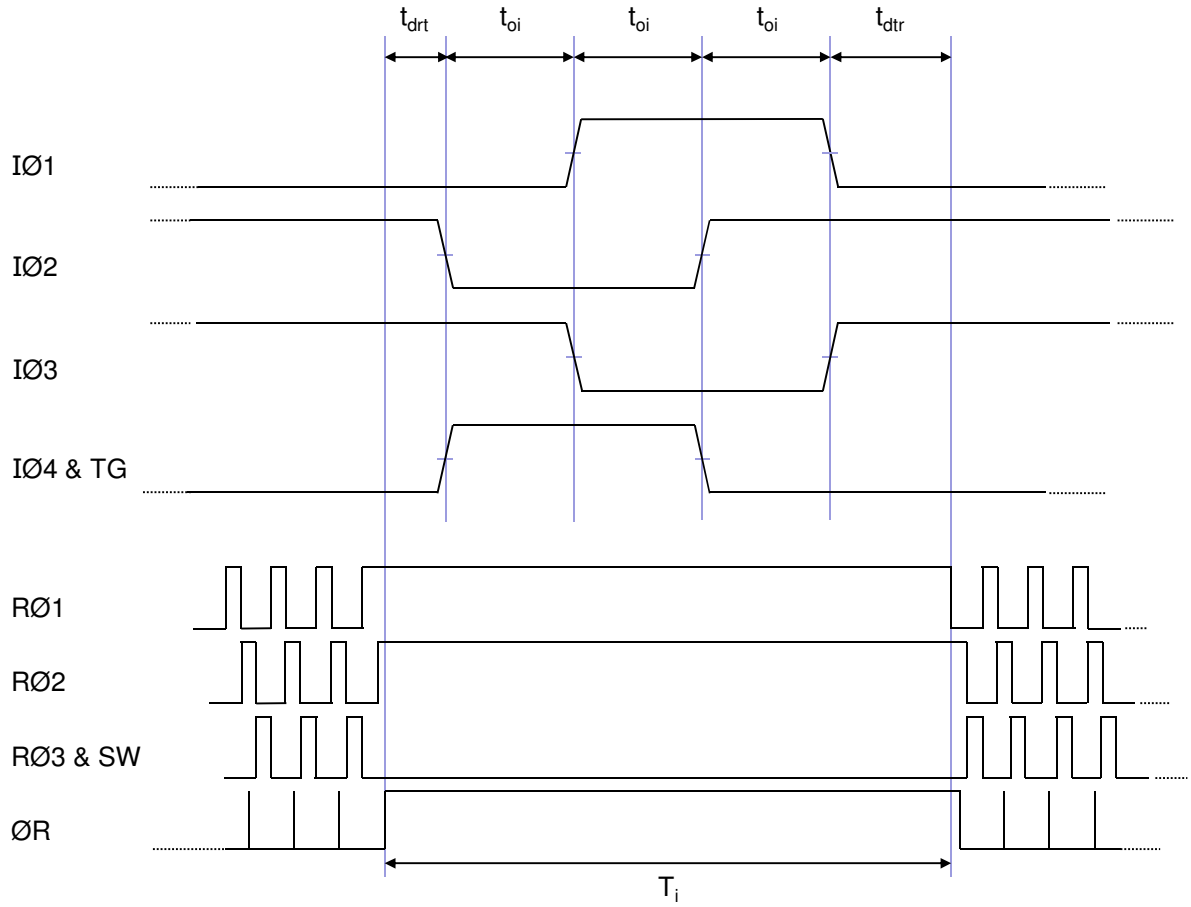
Image phases 2 and 3 should be held high during signal collection, as shown in the following figures.

The register is provided with an anti-blooming dump drain to limit the peak signal capacity. For charge dumping purposes rows of charge signals may be clocked into the register sections and any excess charge above full-well capacity spills into the drain. There must then be a single line read-out to remove the unwanted charge (i.e. which can be up to the full-well capacity) before transferring the wanted row or rows of charge signals into the register sections. However, please see note 13 above also.

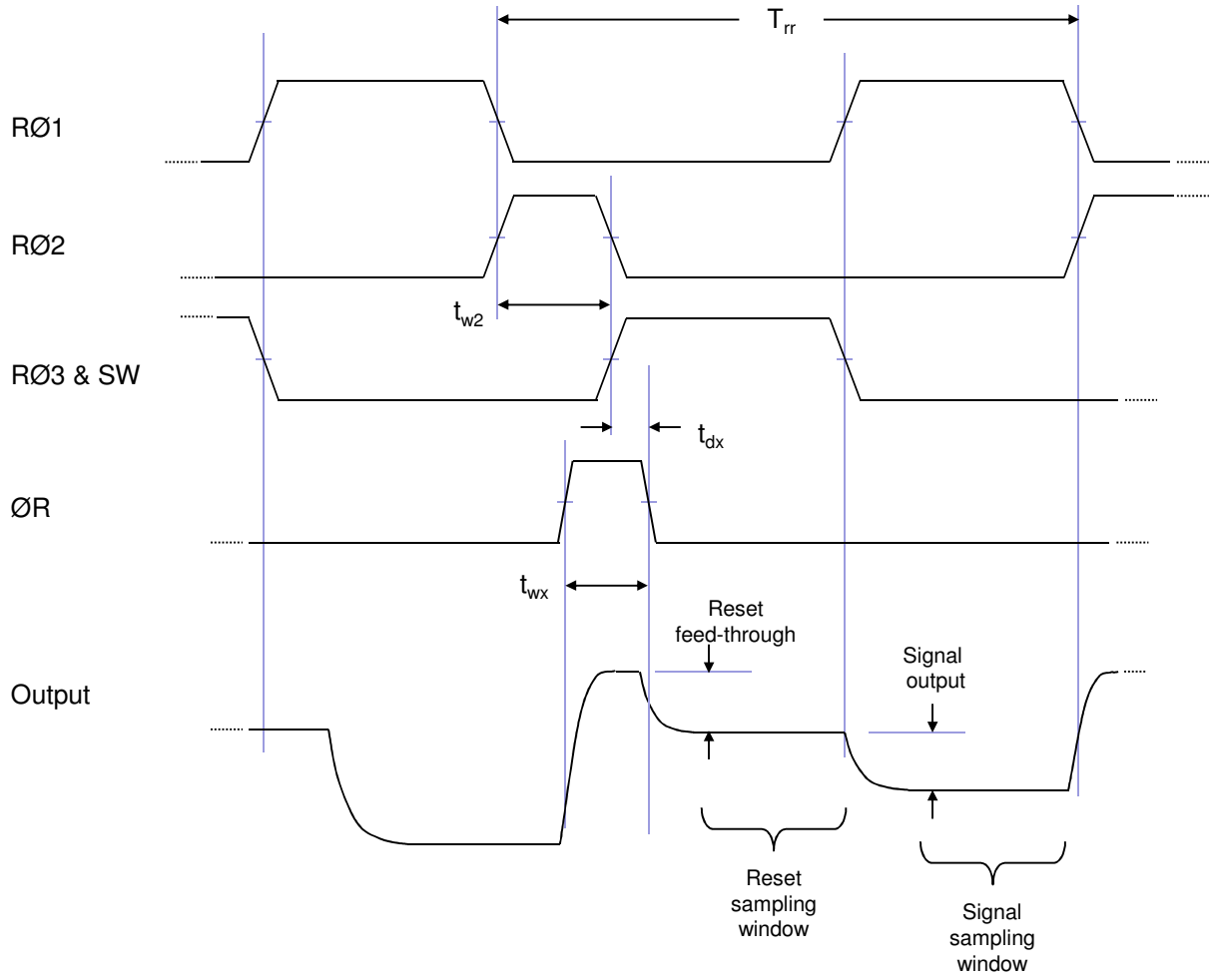
FRAME READ-OUT TIMING DIAGRAM

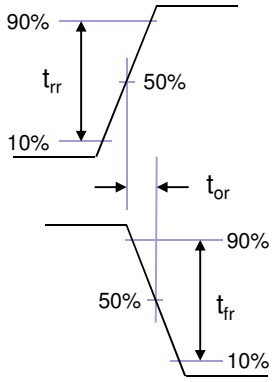


DETAIL OF LINE TRANSFER

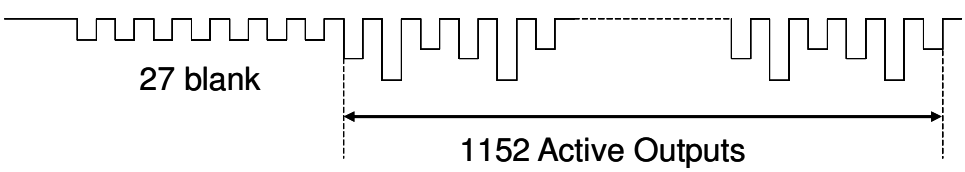


DETAIL OF OUTPUT CLOCKING (with SW clocked as RØ3)





LINE OUTPUT FORMAT



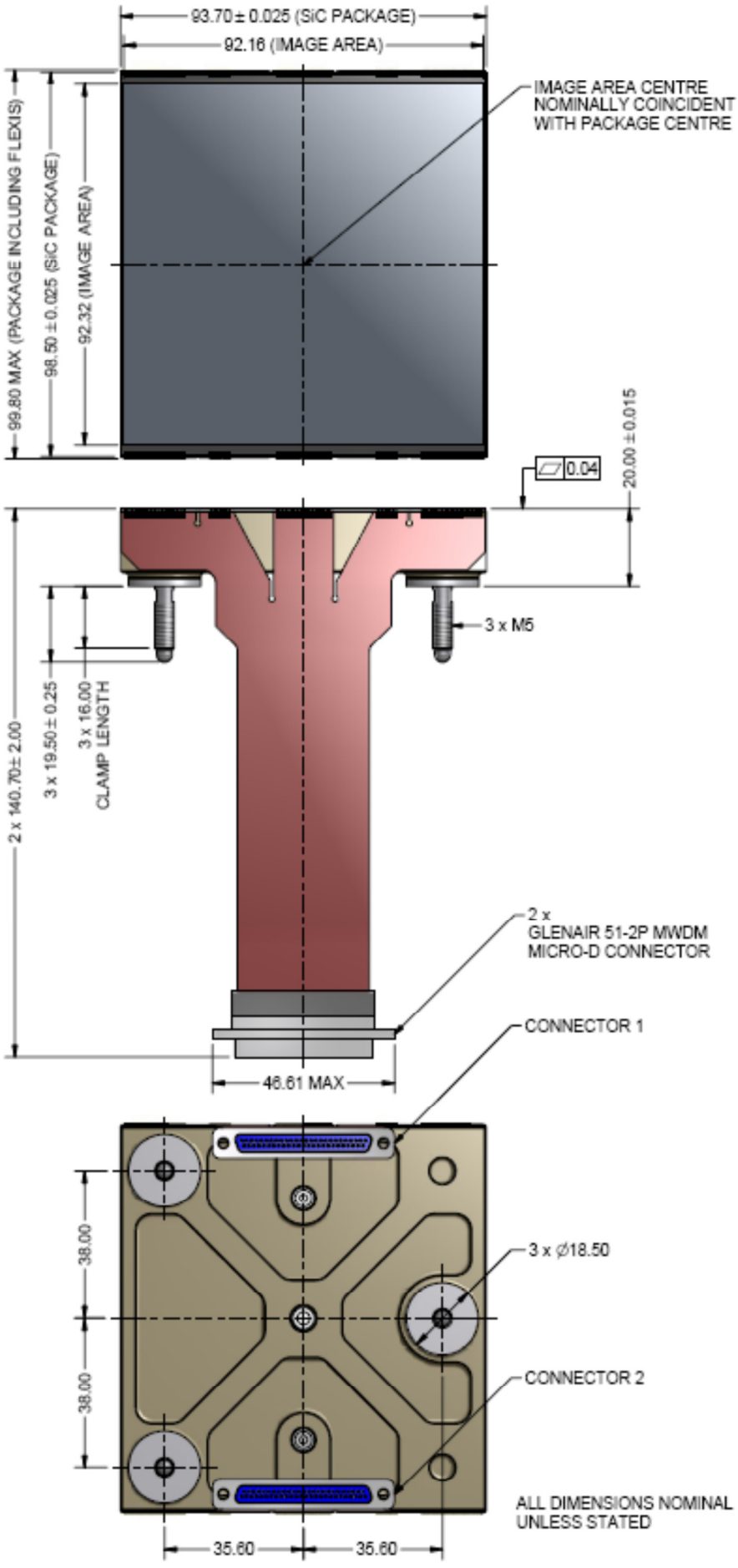
CLOCK TIMING REQUIREMENTS

Symbol	Description	Minimum	Typical	Maximum	Units
T_i	Line transfer time (see note 14)	120	300		µs
t_{oi}	Image clock pulse edge overlap (see note 15)	25	30		µs
t_{ri}	Image clock and transfer gate pulse rise time	2	5	0.3 t_{oi}	µs
t_{fi}	Image clock and transfer gate pulse fall time	2	5	0.3 t_{oi}	µs
t_{drt}	Delay time, RØ stop to IØ rising	15	30		µs
t_{dtr}	Delay time, IØ falling to RØ start	30	80		µs
T_{rr}	Register clock period (see note 16)	300	2000	(see note 17)	ns
t_{w2}	RØ2 pulse width at 50% levels (see note 18)	$3t_{rx}$	350	$T_{rr}/3$	ns
t_{rr}	Register clock pulse rise time	10	50	$0.05T_{rr}$	ns
t_{fr}	Register clock pulse fall time	10	50	$0.05T_{rr}$	ns
t_{or}	Register clock pulse edge overlap at 50% levels	0	50	$0.05T_{rr}$	ns
t_{wx}	Reset pulse width at 50% levels	3 t_{rx}	300	$0.2T_{rr}$	ns
t_{rx}	Reset pulse rise time	10	40	$0.2t_{wx}$	ns
t_{fx}	Reset pulse fall time	10	40	$0.2t_{wx}$	ns
t_{dx}	Delay time, RØ falling to ØR falling	10	100	$0.05T_{rr}$	ns

NOTES

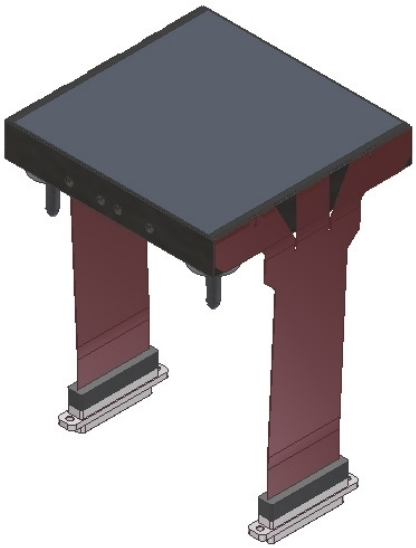
14. Generally $T_i = t_{drt} + 3t_{oi} + t_{dtr}$.
15. The IØ1/IØ3, IØ2/IØ4, IØ3/IØ1 and IØ4/IØ2 transitions are nominally coincident with the edges overlapping at 50% amplitude.
16. The typical timing is for readout at frequencies in the region of 500 kHz, as used for factory tests.
17. For highest speed operation the output load resistor can be reduced from 5 kΩ to approximately 2.2 kΩ, but note that this will increase power consumption. If the device is to be operated with a register clock period of below about 1 MHz, then the load may be increased to 10 kΩ to reduce power consumption.
18. The RØ2 pulse-width is normally minimised, as shown, such that the RØ1 and RØ3 pulse widths can be increased to maximise the output reset and signal sampling intervals.

PACKAGE DETAIL



The package base is Silicon Carbide; fitted with two flex-cable connectors and three mounting studs.

Interface drawing DAS772494AT (available on request) provides further information



HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases, a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving sockets to be positively grounded

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (i.e. all CCD pins except SS, DD, RD, OD and OS) but not to the other pins.

The devices are assembled in a clean room environment. e2v technologies recommend that similar precautions are taken to avoid contaminating the active surface.

Buttable flex-cable devices require careful handling to avoid damage to silicon, bond wires of flex cables. Avoid stress on flex cables, and contact factory for advice if needed.

HIGH ENERGY RADIATION

Performance parameters will begin to change if the device is subject to ionising radiation. Characterisation data is held at e2v technologies with whom it is recommended that contact be made if devices are to be operated in any high radiation environment.

TEMPERATURE RANGE

Operating temperature range 153 - 323 K

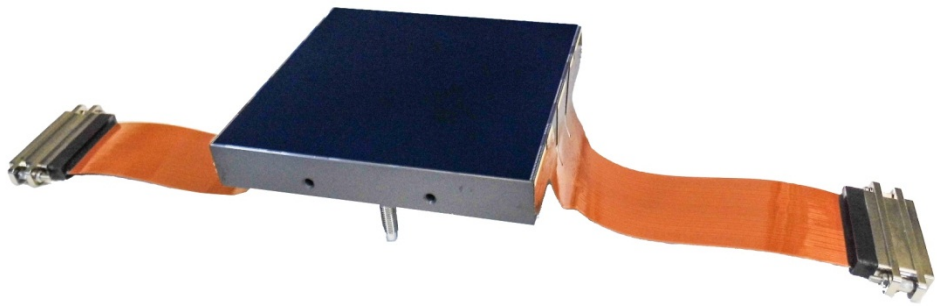
Storage temperature range 148 - 358 K

Performance parameters are measured with the device at a temperature of 173 K and, as a result, full performance is only guaranteed at this nominal operating temperature.

Operation or storage in humid conditions before the sensor taken to low ambient temperatures may give rise to ice on the surface, thereby causing irreversible damage.

Maximum rate of heating or cooling: 5 K/min

CCD290-99 Back Illuminated Scientific CCD Sensor
9216 x 9232 Pixels, Sixteen Outputs
Non-inverted Mode Operation



INTRODUCTION

The CCD290 extends e2v's family of scientific CCD sensors and has been designed to provide a large image area for demanding astronomical and scientific imaging applications. Back-illuminated spectral response combined with very low read-out noise give exceptional sensitivity.

DESCRIPTION

The sensor has an image area having 9216 × 9232 pixels with registers at both top and bottom each with eight outputs for short read-out times. The pixel size is 10 µm square. The image area has two separately connected sections to allow full-frame or split full-frame read-out modes. Depending on the mode, the read-out can be through 8 or 16 of the output circuits. A fixed-barrier dump drain is also provided to allow fast dumping of unwanted data.

The output amplifier is designed to give very low noise at read-out rates of up to 3 MHz. The low output impedance simplifies the interface with external electronics and the optional dummy outputs are provided to facilitate common mode rejection.

The package provides a compact footprint with guaranteed flatness at cryogenic temperatures. Connections are made at the top and bottom of the device via two flexi connectors that also provide a thermal break. The sides may be close butted if needed.

Specifications are tested and guaranteed at 173K (–100 °C).

The CCD290 is a non-inverted (non-MPP) type.

VARIANTS

Standard silicon and deep-depletion silicon device types can be supplied with a range of AR coatings. Graded coatings and two-layer coatings are available as custom variants.

Devices with other formats (e.g. 4608 × 4608, or 6144 × 6144 pixels) or fewer outputs (4 or 8) may also be available to custom order.

Consult e2v technologies for further information on any of the above options.

SUMMARY PERFORMANCE (Typical)

Number of pixels	9216 (H) × 9232 (V)
Pixel size	10 µm square
Image area	92.2 mm × 92.4 mm
Outputs	16
Package size	98.5 × 93.7 mm
Package format	Silicon carbide with two flexi connectors
Focal plane height, above base	20.0 mm
Height tolerance	±15 µm
Connectors	Two 51-way micro-D
Flatness	<40 µm (peak to valley)
Amplifier sensitivity	7 µV/e^-
Read-out noise	4 e^- at 0.5 MHz 2.5 e^- at 50 kHz
Maximum pixel data rate	3 MHz
Charge storage (pixel full well)	90,000 e^-
Dark signal	2 e^-/pixel/hour (at –100 °C)

Quoted performance parameters given here are "typical" values. Specification limits are shown later.

Part References

CCD290-99-g-xxx

g = cosmetic grade
xxx = device-specific part number

CCD290-99-1-F24 Grade-1, deep depletion, astro multi-2

CCD290-99-1-F81 Grade-1, deep depletion, astro multi-7

CCD290-99-1-F82 Grade-1, standard silicon, astro multi-2

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Template: DF764388A-2
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PERFORMANCE (At 173K unless stated)

Electro-Optical Specification (CCD290 Normal Mode, see note 1)

	Min	Typical	Max	Units	Note
Peak charge storage (image pixel)	70,000	90,000	-	e^-/pixel	2(a)
Peak charge storage (register SW)	-	140,000	-	e^-/pixel	2(b)
Output node capacity: OG low mode 1 OG high mode 2 (not factory tested)	 - -	 240,000 700,000	 - -	 e^- e^-	2(c)
Output amplifier responsivity: mode 1 mode 2 (not factory tested)	 5.0 -	 7.0 2.5	 - -	 µV/e^- µV/e^-	3
Read-out noise 50 kHz (not factory tested) 500 kHz	 -	 2.5 4	 - 7	e^- rms	4
Maximum read-out frequency	-	1000	3000	kHz	5
Dark signal: at 173 K at 153 K	 - -	 2 0.02	 - 2.0	 e^-/pixel/hr e^-/pixel/hr	6
Charge transfer efficiency: parallel serial	 99.9990 99.9990	 99.9995 99.9995	 100 100	 % %	7
Spectral range	300	-	1060	nm	
Peak quantum efficiency	-	90	-	%	

NOTES

1. Device performance will be within the limits specified by “max” and “min” when operated at the recommended voltages supplied with the test data and when measured at a register clock frequency of approximately 0.1 – 1.0 MHz. Acceptance tests are performed at a nominal 500 kHz pixel rate.
2. (a) Signal level at which resolution begins to degrade. Device is non-inverted (NIMO/non-MPP), for maximum full well.

   (b) The summing well capacity limits the charge in the register. The limiting value may change in mode-2 but is not tested.

   (c) The signal handled by the output node (for linear operation) varies with mode as shown.
3. Under normal operation (mode 1), SW is operated as a summing well or clocked as RØ3. OG is biased at a low DC level.

   Alternatively (mode 2), SW may be operated as an output gate (and not therefore available for summing) and biased at a low DC level with OG raised to a high voltage (see note 9 later). This gives more charge-handling capacity (e.g. for higher level pixel binning). Charge transfer to the output now occurs as RØ2 goes low. In mode-2, the output noise will also increase by a factor of three. Mode-2 is not factory tested.
4. Noise is specified and measured using correlated double sampling at 500 kHz nominal read-out rate in mode 1 only. Performance at 50 kHz is also indicated (but not production-tested). If real and dummy outputs are used, differential noise is $\sqrt{2}$ higher.
5. The register will transfer charge at higher frequencies, depending on the external load capacitance to be driven, but performance cannot be guaranteed.
6. Dark signal is typically measured at a device temperature of 173 K. It is a strong function of temperature and the typical average (background) dark signal at any temperature T (kelvin) between 150 K and 300 K is given by:

   $Q_d/Q_{do} = 122T^3e^{-6400/T}$

   where Q_{do} is the dark current at 293 K.

   Note that this is typical performance and some variation may be seen between devices.
7. Measured with a ^{55}Fe X-ray source. The CTE value is quoted for the complete clock cycle (i.e. not per phase).

SPECTRAL RESPONSE

The table below gives guaranteed minimum values of the spectral response for several variants. PRNU is also shown.

Standard Silicon Devices

	Standard silicon Astro Broadband	Standard silicon Astro Midband	Standard silicon Astro Multi-2	Maximum Pixel Response Non-Uniformity PRNU (1 σ) (%)
Wavelength (nm)	**Minimum QE (%)**	**Minimum QE (%)**	**Minimum QE (%)**	
350	40	20	30	-
400	70	50	75	3
500	80	80	75	-
650	75	80	80	3
900	25	25	25	5

Deep Depletion Devices

	Deep depletion silicon Astro Broadband	Deep depletion silicon Astro Midband	Deep depletion silicon Astro ER1 response	Deep depletion silicon Astro Multi-2	Deep depletion silicon Astro Multi-7	Maximum Pixel Response Non-Uniformity PRNU (1 σ) (%)
Wavelength (nm)	**Minimum QE (%)**	**Minimum QE (%)**	**Minimum QE (%)**	**Minimum QE (%)**	**Minimum QE (%)**	
350	40	20	20	30	-	-
400	70	50	35	75	45	3
500	75	80	65	75	75	-
650	70	80	80	80	80	3
900	40	40	45	50	50	5

Notes

The multi-AR coatings are currently considered as pre-production types prior to full process release. Contact e2v for further details and to discuss their suitability for specific applications.

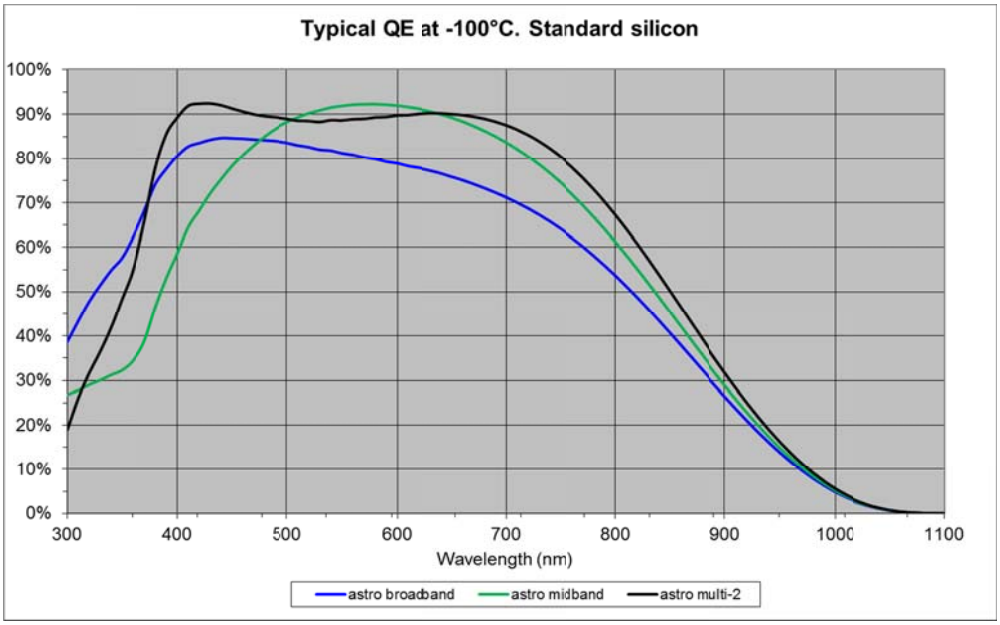
The multi-2 coating is designed for wide-range use.

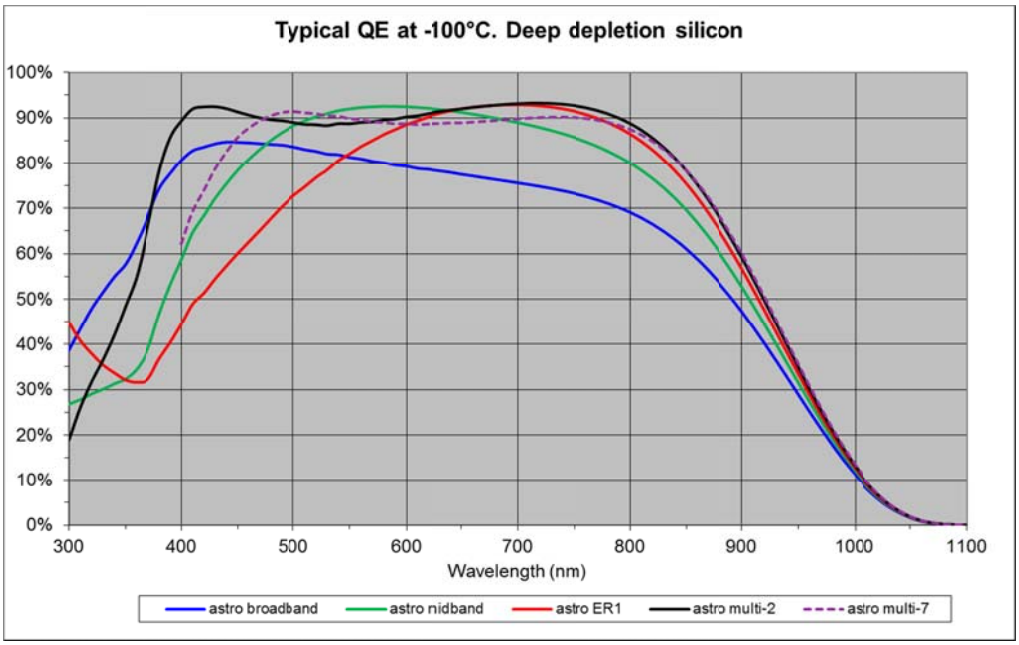
The multi-7 coating is designed specifically for the 500 to 1000 nm region; it has lower reflectivity (and fringing) than the multi-2 coating at the longest wavelengths.

Availability of coatings varies depending on type; check with factory.
Devices with an alternate spectral response may be available. Consult e2v technologies.

See also the typical spectral response figures below.

TYPICAL SPECTRAL RESPONSE CURVES





COSMETIC SPECIFICATIONS

Maximum allowed defect levels are indicated below.

	Guaranteed Specifications			Typical Values		
Grade	**0**	**1**	**2**	**0**	**1**	**2**
Column defects - black or white	10	20	30	2	4	6
White spots	1000	2000	3000	<500	<1000	<1500
Total (black & white) spots	2000	4000	6000	<1000	<2000	<3000
Traps > 200e-	20	30	40	<10	<20	<30

Grade 1 is the default for general science use; consult the factory for grade-0 or grade-2availability.

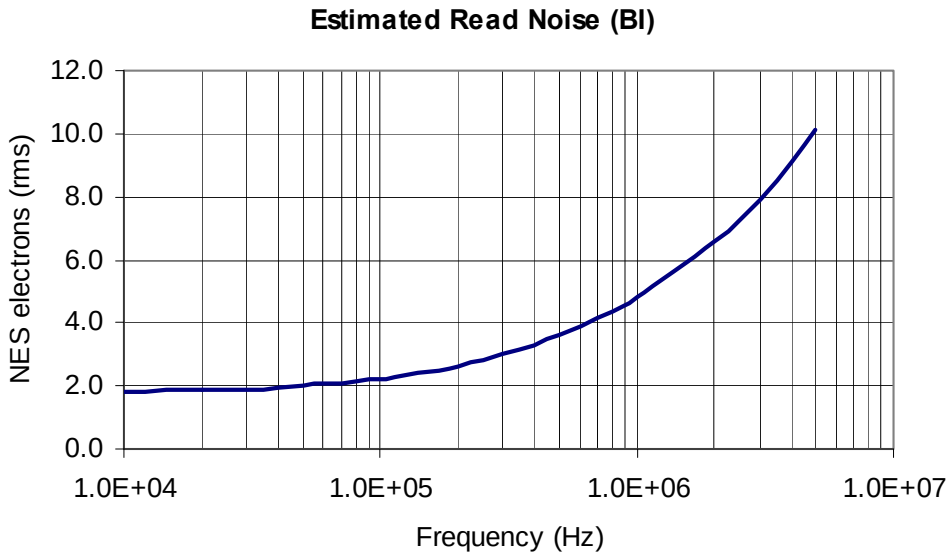
Grade 5 devices may also be available for set-up purposes. These are fully functional but with an image quality below that of grade 2, and may not meet all other specifications. Not all parameters may be tested.

DEFINITIONS

White spots	A defect is counted as a white spot if the dark generation rate is ≥ 5 e^-/pixel/s at 173 K. (which is also equivalent to ≥100 e^-/hour at 153 K). The temperature dependence is the same as for the mean dark signal; see note 6 above.
Black spots	A black spot defect is a pixel with a photo-response less than 50% of the local mean.
Column defects	A column is counted as a defect if it contains at least 100 white or dark single pixel defects.
Traps	A trap causes charge to be temporarily held in a pixel and these are counted as defects if the quantity of trapped charge is greater than 200 e^- at the specified test temperature.
Defect exclusion zone	Defect measurements are excluded from the outer two rows and columns of the sensor.

AMPLIFIER READ NOISE

The modelled variation of typical output amplifier read noise with operating frequency is shown below. This assumes correlated double sampling with a pre-sampling bandwidth equal to twice the pixel rate in mode 1, temperature range 150 – 230 K.



DEFINITIONS

Back-Thinning

A back-thinned CCD is fabricated on the front surface of the silicon and is subsequently processed for illumination from the reverse side. This avoids loss of transmission in the electrode layer (which can be particularly significant at shorter wavelengths or with low energy X-rays). This process requires the silicon to be reduced to a thin layer by a combination of chemical and mechanical means. The surface is “passivated” and an anti-reflection coating may be added.

AR Coating

Anti-reflection coatings are normally applied to the back illuminated CCD to further improve the quantum efficiency. Standard coatings optimise the response in the visible, ultra-violet or infrared regions. For X-ray detection an uncoated device may be preferable.

Read-out Noise

Read-out noise is the random noise from the CCD output stage in the absence of signal. This noise introduces a random fluctuation in the output voltage that is superimposed on the detected signal.

The method of measurement involves reverse-clocking the register and determining the standard deviation of the output fluctuations, and then converting the result to an equivalent number of electrons using the known amplifier responsivity.

Dummy Output

Each output has an associated “dummy” circuit on-chip, which is of identical design to the “real” circuit but receives no signal charge. The dummy output should have the same levels of clock feed-through, and can thus be used to suppress the similar component in the “real” signal output by means of a differential pre-amplifier. The penalty is that the noise is increased by a factor of $\sqrt{2}$. If not required the dummy outputs may be powered down.

Dark Signal

This is the output signal of the device with zero illumination. This typically consists of thermally generated electrons within the semiconductor material, which are accumulated during signal integration. Dark signal is a strong function of temperature as described in note 6.

Correlated Double Sampling

A technique for reducing the noise associated with the charge detection process by subtracting a first output sample taken just after reset from a second sample taken with charge present.

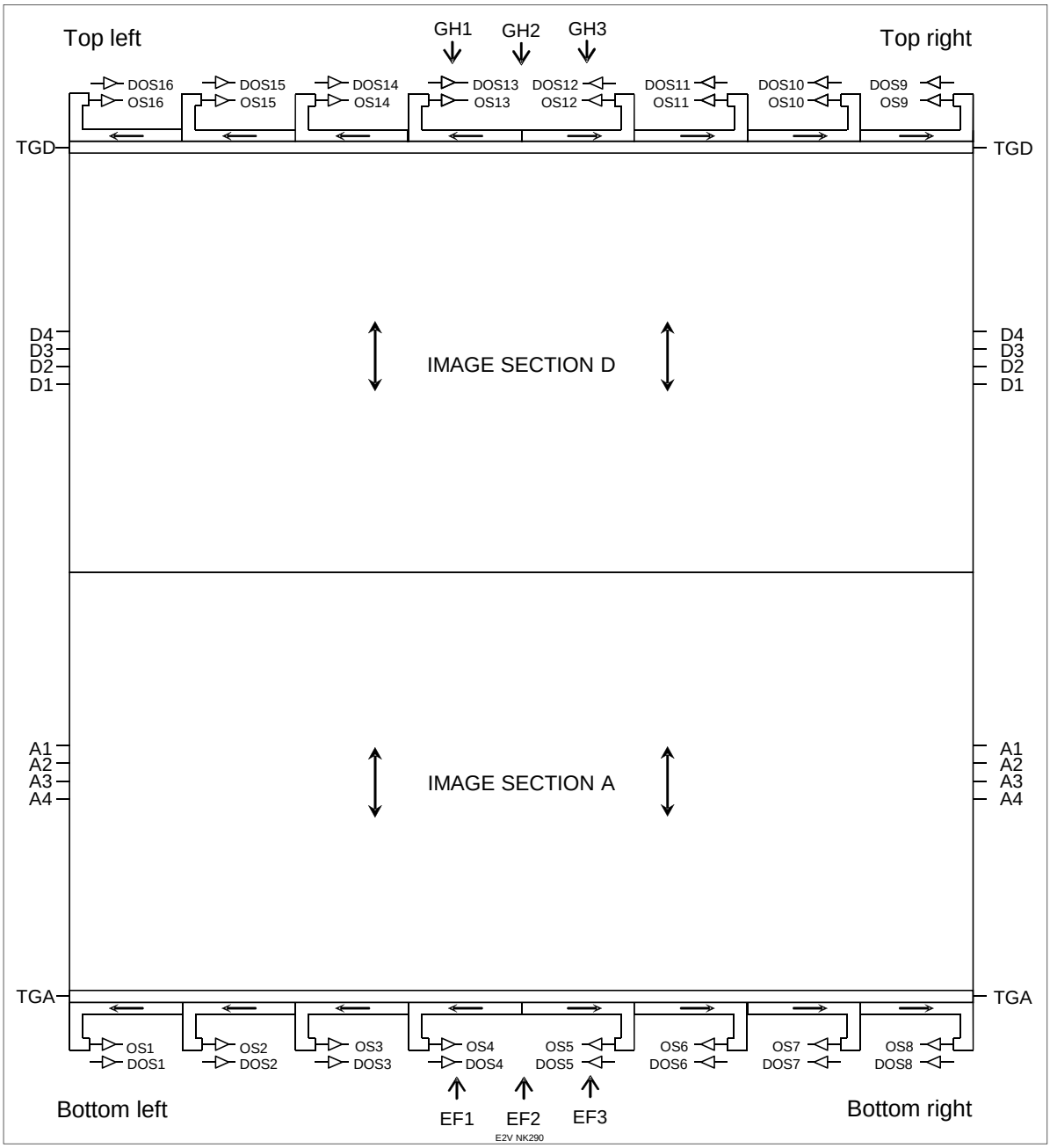
Charge Transfer Efficiency

The fraction of charge stored in a CCD element that is transferred to the adjacent element by a single clock cycle. The charge not transferred remains in the original element, possibly in trapping states and may possibly be released into later elements. The value of CTE is not constant but varies with signal size, temperature and clock frequency.

ARCHITECTURE

Chip Schematic

TOP



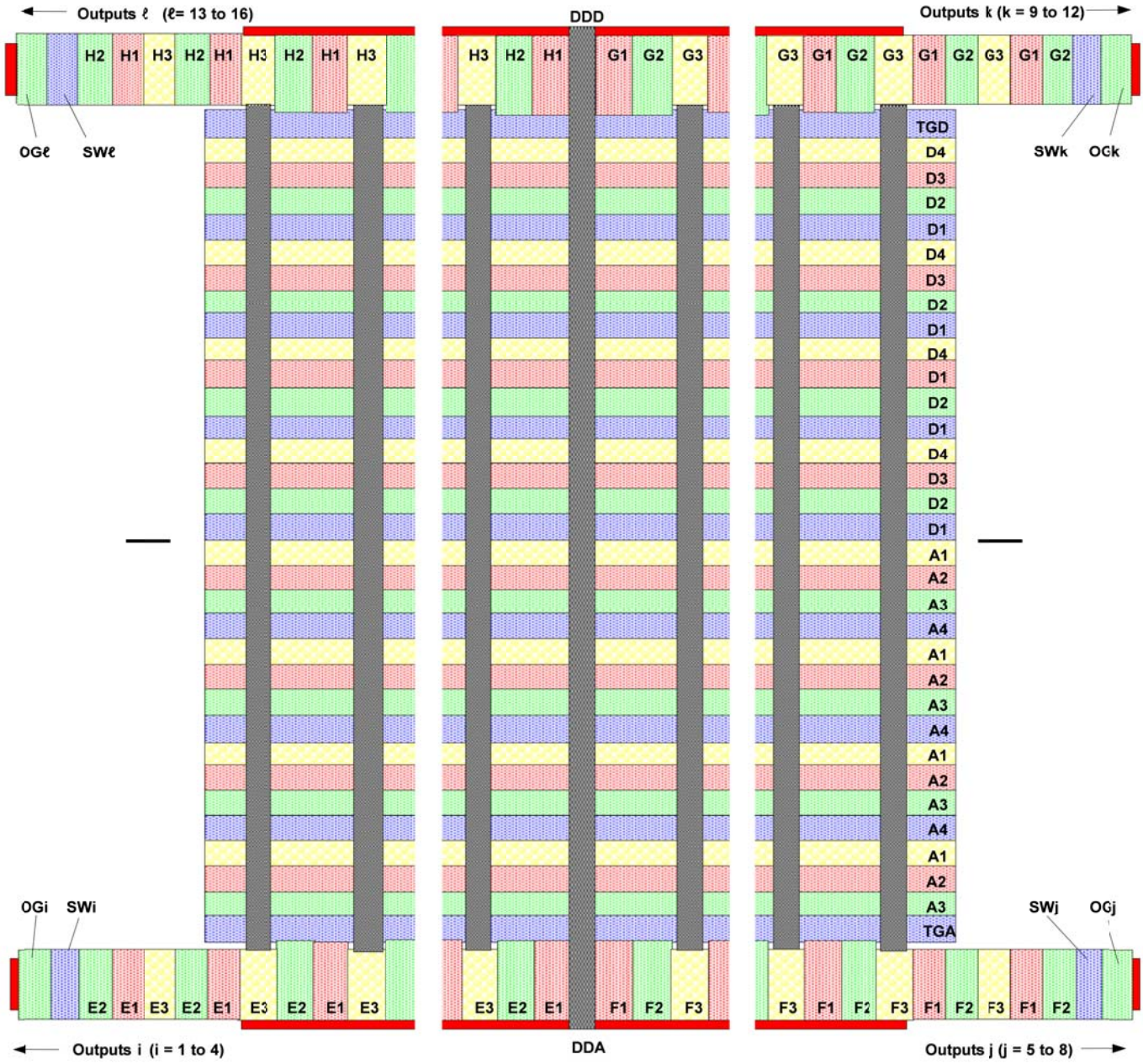
BOTTOM

Image sections A and D each have a total of 9216 (H) × 4616 (V) pixels.

Each register section has a total of 1179 elements: 1152 active and 27 pre-scan.

Connector-1 (and flexi) is at the “bottom” of the device (register EF); Connector-2 is at the “top” of the device (register GH).

ARRANGEMENT OF ELECTRODES

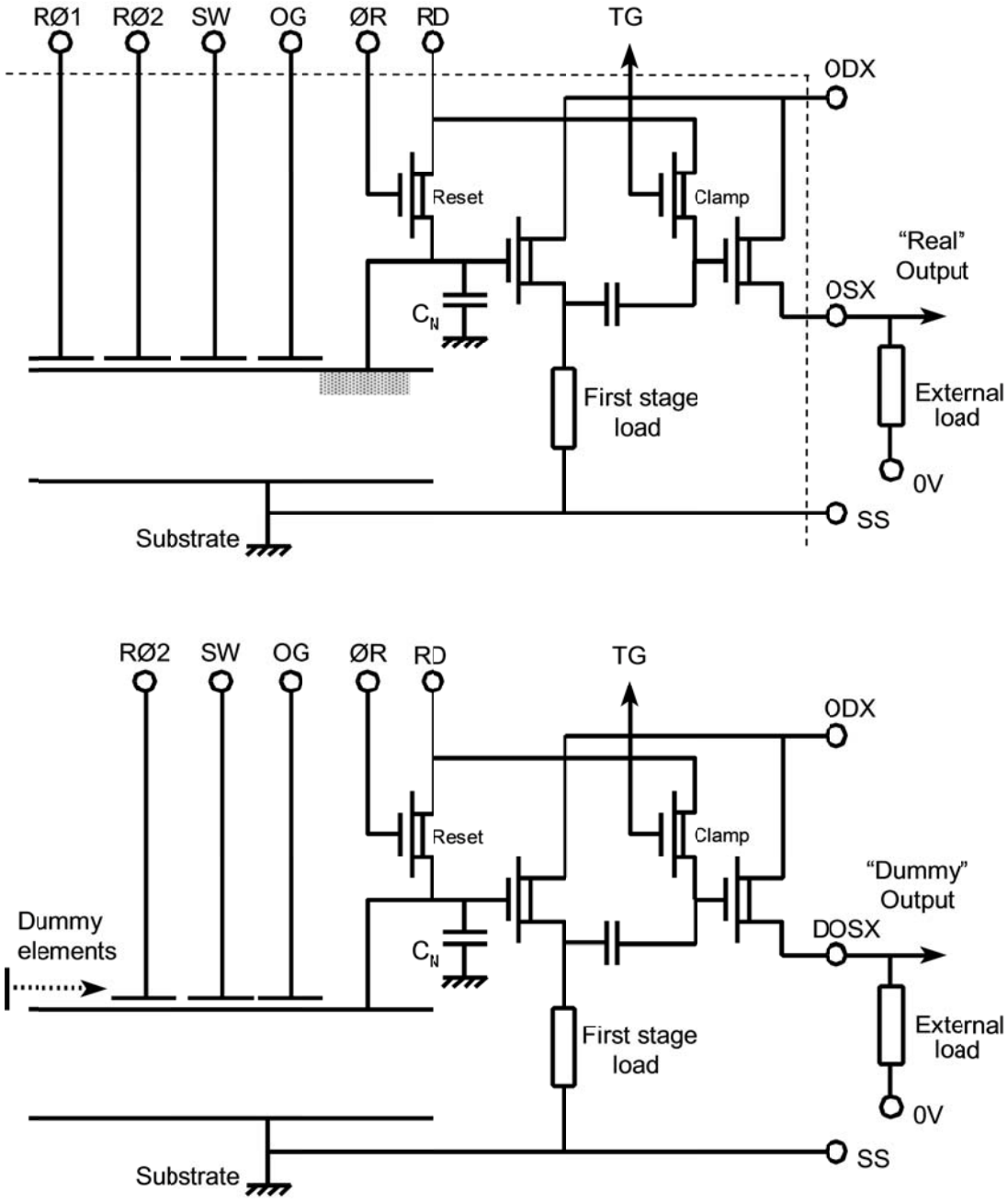


Pre-scan (blank) serial elements are not shown here.

Each output consists of real (OS) and dummy (DOS); see next page.

OUTPUT CIRCUIT

X designates a specific output, namely 1 to 16 (see the chip schematic).



The first stage load of each output (real or dummy) draws a quiescent current of approximately 0.2 mA via SS.

The output circuit consists of two capacitor-coupled source-follower stages. The particular design has a very high responsivity to give lowest noise. The load for the first stage is on-chip and that for the second stage is external, as next described. The DC restoration circuitry requires a pulse at the start of line readout, and this is automatically obtained by an internal connection to the adjacent transfer gate, TG. Transferring a line of charges to the register thus automatically activates the circuitry. TG pulses still need to be applied at similar intervals if only the register and/or output circuit are being operated, e.g. for test or characterisation purposes.

The amplifier output impedance is typically 400 Ω.

ELECTRICAL INTERFACES

CONNECTOR 1

PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (See note 10)			MAX RATINGS (V) with respect to V_{SS}
			Min	Typical	Max	
1	A1	Image Area A Clock Phase 1	9	11	12	±20
2	A2	Image Area A Clock Phase 2	9	11	12	±20
3	TGA	Image Area A Transfer gate	9	11	12	±20
4	OD1	Output Drain 1	25	29	31	-0.3 to +35
5	OS1	Output Source 1		(see note 8)		
6	OD2	Output Drain 2	25	29	31	-0.3 to +35
7	OS2	Output Source 2		(see note 8)		
8	OD3	Output Drain 3	25	29	31	-0.3 to +35
9	OS3	Output Source 3		(see note 8)		
10	OD4	Output Drain 4	25	29	31	-0.3 to +35
11	OS4	Output Source 4		(see note 8)		
12	SS	Substrate (see note 11)	0	0	10	N/A
13	ØRA	Reset Gate (A) (See note 12)	9	12	13	±20
14	SWA	Summing Well (A) (See note 9)	9	10	12	±20
15	SS	Substrate (see note 11)	0	0	10	N/A
16	OS5	Output Source 5		(see note 8)		
17	OD5	Output Drain 5	25	29	31	-0.3 to +35
18	OS6	Output Source 6		(see note 8)		
19	OD6	Output Drain 6	25	29	31	-0.3 to +35
20	OS7	Output Source 7		(see note 8)		
21	OD7	Output Drain 7	25	29	31	-0.3 to +35
22	OS8	Output Source 8		(see note 8)		
23	OD8	Output Drain 8	25	29	31	-0.3 to +35
24	TGA	Image Area A Transfer Gate	9	11	12	±20
25	A2	Image Area A Clock Phase 2	9	11	12	±20
26	A1	Image Area A Clock Phase 1	9	11	12	±20
27	A3	Image Area A Clock Phase 3	9	11	12	±20
28	A4	Image Area A Clock Phase 4	9	11	12	±20
29	RD1/2	Reset Drain (1/2)	16	17	19	-0.3 to +25
30	DOS1	Dummy Output Source 1		(see note 8)		
31	SS	Substrate (see note 11)	0	0	10	N/A
32	DOS2	Dummy Output Source 2		(see note 8)		
33	RD 3/4	Reset Drain (3/4)	16	17	19	-0.3 to +25
34	DOS3	Dummy Output Source 3		(see note 8)		
35	SS	Substrate (see note 11)	0	0	10	N/A
36	DOS4	Dummy Output Source 4		(see note 8)		
37	OGA	Output Gate (A) (See note 9)	1	2	(note 9)	±20
38	E3/F3	Register E & Register F Clock Phase 3	9	10	12	±20
39	E2/F2	Register E & Register F Clock Phase 2	9	10	12	±20
40	E1/F1	Register E & Register F Clock Phase 1	9	10	12	±20
41	DDA	Dump Drain (A) (See note 13)	15	18	20	-0.3 to +35
42	DOS5	Dummy Output Source 5		(see note 8)		
43	SS	Substrate (see note 11)	0	0	10	N/A
44	DOS6	Dummy Output Source 6		(see note 8)		
45	RD5/6	Reset Drain (5/6)	16	17	19	-0.3 to +25
46	DOS7	Dummy Output Source 7		(see note 8)		
47	SS	Substrate (see note 11)	0	0	10	N/A
48	DOS8	Dummy Output Source 8		(see note 8)		
49	RD7/8	Reset Drain (7/8)	16	17	19	-0.3 to +25
50	A4	Image Area A Clock Phase 4	9	11	12	±20
51	A3	Image Area A Clock Phase 3	9	11	12	±20

CONNECTOR 2

PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (See note 10)			MAX RATINGS (V) with respect to V_{SS}
			Min	Typical	Max	
1	D4	Image Area D Clock Phase 4	9	11	12	±20
2	D3	Image Area D Clock Phase 3	9	11	12	±20
3	TGD	Image Area D Transfer gate	9	11	12	±20
4	OD9	Output Drain 9	25	29	31	-0.3 to +35
5	OS9	Output Source 9		(see note 8)		
6	OD10	Output Drain 10	25	29	31	-0.3 to +35
7	OS10	Output Source 10		(see note 8)		
8	OD11	Output Drain 11	25	29	31	-0.3 to +35
9	OS11	Output Source 11		(see note 8)		
10	OD12	Output Drain 12	25	29	31	-0.3 to +35
11	OS12	Output Source 12		(see note 8)		
12	SS	Substrate (see note 11)	0	0	10	N/A
13	ØRD	Reset Gate (D) (See note 12)	9	12	13	±20
14	SWD	Summing Well (D) (See note 9)	9	10	12	±20
15	SS	Substrate (see note 11)	0	0	10	N/A
16	OS13	Output Source 13		(see note 8)		
17	OD13	Output Drain 13	25	29	31	-0.3 to +35
18	OS14	Output Source 14		(see note 8)		
19	OD14	Output Drain 14	25	29	31	-0.3 to +35
20	OS15	Output Source 15		(see note 8)		
21	OD15	Output Drain 15	25	29	31	-0.3 to +35
22	OS16	Output Source 16		(see note 8)		
23	OD16	Output Drain 16	25	29	31	-0.3 to +35
24	TGD	Image Area D Transfer Gate	9	11	12	±20
25	D3	Image Area D Clock Phase 3	9	11	12	±20
26	D4	Image Area D Clock Phase 4	9	11	12	±20
27	D2	Image Area D Clock Phase 2	9	11	12	±20
28	D1	Image Area D Clock Phase 1	9	11	12	±20
29	RD9/10	Reset Drain (9/10)	16	17	19	-0.3 to +25
30	DOS9	Dummy Output Source 9		(see note 8)		
31	SS	Substrate (see note 11)	0	0	10	N/A
32	DOS10	Dummy Output Source 10		(see note 8)		
33	RD11/12	Reset Drain (11/12)	16	17	19	-0.3 to +25
34	DOS11	Dummy Output Source 11		(see note 8)		
35	SS	Substrate (see note 11)	0	0	10	N/A
36	DOS12	Dummy Output Source 12		(see note 8)		
37	OGD	Output Gate (D) (See note 9)	1	2	(note 9)	±20
38	G3/H3	Register G & Register H Clock Phase 3	9	10	12	±20
39	G1/H1	Register G & Register H Clock Phase 1	9	10	12	±20
40	G2/H2	Register G & Register H Clock Phase 2	9	10	12	±20
41	DDD	Dump Drain (D) (See note 13)	15	18	20	-0.3 to +35
42	DOS13	Dummy Output Source 13		(see note 8)		
43	SS	Substrate (see note 11)	0	0	10	N/A
44	DOS14	Dummy Output Source 14		(see note 8)		
45	RD13/14	Reset Drain (13/14)	16	17	19	-0.3 to +25
46	DOS15	Dummy Output Source 15		(see note 8)		
47	SS	Substrate (see note 11)	0	0	10	N/A
48	DOS16	Dummy Output Source 16		(see note 8)		
49	RD15/16	Reset Drain (15/16)	16	17	19	-0.3 to +25
50	D1	Image Area D Clock Phase 1	9	11	12	±20
51	D2	Image Area D Clock Phase 2	9	11	12	±20

NOTES

8. Do not connect to voltage supply but use a ~5 mA current source or a ~5 kΩ external load. The quiescent voltage on OS is then about 6 - 8 V above the reset drain voltage and is typically 24 V. The current through these pins must not exceed 20 mA. Permanent damage may result if, in operation, OS or DOS experience short circuit conditions.

   For highest speed operation the output load resistor can be reduced from 5 kΩ to approximately 2.2 kΩ, but note that this will increase power consumption. If the device is to be operated with a register clock period of below about 1 MHz then the load may be increased to 10 kΩ to reduce power consumption.

9. Default operation (mode 1) shown with OG set to OG-Low, with a +2 V nominal value. In this mode SW may be clocked as RØ3 if a summing well function is not required. OG-Low should have a maximum value of +5 V.

   For alternative operation in a low responsivity mode (mode 2) with increased charge handling, OG should be set to OG-High and SW should be operated as OG-Low (i.e. 2V typical). See below for appropriate OG-High values. Charge is now read out as RØ2 goes low.

   See note 11 also for discussion about Substrate voltage (Vss). With high substrate voltage OG-High may be set to a nominal +20 V, which offers best linearity in mode-2. With low substrate voltage, the allowed maximum value of OG-High is limited to a nominal +18 V; the lower OG-High value has a greater non-linearity.

10. To ensure that any device can be operated the camera should be designed so that any value in the range “min” to “max” can be provided. All operating voltages are with respect to image clock low (nominally 0 V).

    The clock pulse low levels should be in the range 0 ± 0.5 V for image clocks. The register and SW clock low level should be +1 V higher. Reset clock low may be nominally 0 V or +1 V.

    In all cases, specific recommended settings will be supplied with each science-grade sensor.

11. The substrate voltage (Vss) has a default value of 0 V (“low” substrate). This is particularly recommended for deep-depletion device variants, since it optimises depletion depth for best Point Spread Function. Devices may alternatively be operated at “high” substrate, with Vss = 9 V. The high substrate setting offers slightly lower dark current, although this is usually not of primary concern when the device is cryogenically cooled. See also note 19 below, referring to Vss level as prior to readout.

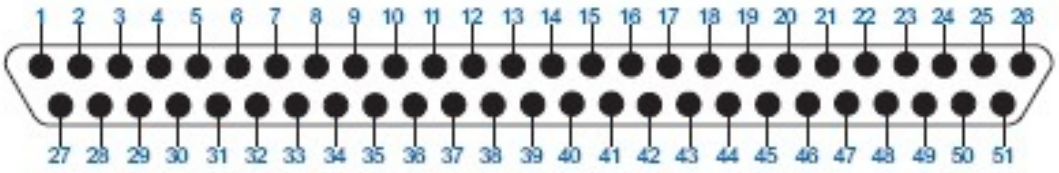
    The substrate setting has some consequence for the allowed OG upper voltage level, as discussed in note 9.

12. Standard silicon variants are expected to be used with ØR at +10 V or more; deep depletion variants require at least +12 V. A higher value will give a correspondingly higher reset feed-through signal in the device output (OS).

13. The DD function may change in future versions. Consult factory for information.

    The DD voltage level determines the level at which register overspill into the drain occurs.

PIN CONNECTIONS (View facing pins of connector)



This numbering applies to both connectors. The connector is a Glenair 51P micro D type.

ELECTRICAL INTERFACE CHARACTERISTICS

Electrode capacitances (defined at mid-clock level)

	Typical	Units
IØ/IØ inter-phase [A, D]	70	nF
IØ/SS per phase [A, D]	20	nF
Total IØ per phase (to Vss and two inter-phase)	160	nF
Transfer gates [TGA, TGD]	150	pF
RØ total per phase [each of E1/F1, G1/H1]	450	pF
RØ total per phase [each of E2/F2, G2/H2]	600	pF
RØ total per phase [each of E3/F3, G3/H3]	650	pF

The total capacitance to be driven per phase is the sum of the component to substrate and the inter-phase components to each of the adjacent phases. With 8 images phases the total parallel capacitance is 1.28 μF. Summing each of the 6 register phase capacitances gives a total serial capacitance of 3.4 nF.

POWER CONSUMPTION

The power dissipated within the CCD is a combination of the static dissipation of the amplifiers and the dynamic dissipation from both of the parallel and serial clocking (i.e. driving the capacitive loads). The dynamic power dissipation (P) is determined separately for the serial and parallel clocking using capacitance, voltage and frequency values via the $P = CV^2f$ relationship. This will be the total clocked power and is divided between the drive buffer (off-chip) and the device (on-chip).

The table below gives representative values for the components of the on-chip power dissipation for the case of continuous split-frame line-by-line readout using both registers and all the output circuits with both real and dummy amplifiers activated. The frequency is that for clocking the serial register and an appropriate value of the amplifier load is utilised in each case.

Read-out frequency	Frame Time	Line read time	Amplifier load	Power dissipation			
				Amplifiers	Serial clocking	Parallel clocking	Total (approx)
0.5 MHz	12.3 s	2.7 ms	5 kΩ	800 mW	~138 mW	~ 58 mW	1.0 W
1 MHz	6.8 s	1.5 ms	5 kΩ	800 mW	~275 mW	~105 mW	1.2 W
3 MHz	3.2 s	0.7 ms	5 kΩ	800 mW	~826 mW	~ 223 mW	1.8 W

Line transfer time and clock amplitudes are taken as the typical values listed in the clock timing requirements and electrical interfaces tables. 1179 register pixels are readout per register section for a total of 4616 rows.

The dissipation reduces to only that of the amplifiers during the time that charge is being collected in the image sections with both the parallel and serial clocks static.

Each flex-cable has a thermal conductivity of approximately 1 mW/°C.

POWER UP/POWER DOWN

When powering the device up or down it is critical that any specified maximum rating is not exceeded. Specifically the voltages for the amplifier and dump drains (OD, RD, DD) must never be taken negative with respect to the substrate. Hence, if the substrate is to be operated at a positive voltage (e.g. to minimise dark current) then the drive electronics should have a switch-on sequence which powers up all the drains to their positive voltages before the substrate voltage starts to increase from zero.

It is also important to ensure that excess currents (see note 8) do not flow in the OS or DOS pins. Such currents could arise from rapid charging of a signal coupling capacitor or from an incorrectly biased DC-coupled preamplifier.

Similarly, for powering down, the substrate must be taken to zero voltage before the drains.

FRAME READ-OUT MODES

The device can be operated in a full-frame or split full-frame mode.

If the applied drive pulses are designated IØ1, IØ2, IØ3 and IØ4, then connections should be made as tabulated below to effect the following directions of transfer.

Clock Generator Drive Pulse Name	IØ1	IØ2	IØ3	IØ4	
A section transfer towards E register	A1	A2	A3	A4	TGA = IØ4
D section transfer towards G register	D1	D2	D3	D4	TGD = IØ1
A section transfer towards G register	A4	A3	A2	A1	TGA = “low”
D section transfer towards E register	D4	D3	D2	D1	TGD = “low”

The first two transfer sequences are for split frame read-out. The second two are for reversing the transfer direction in either section for read-out to either the top or the bottom register sections.

Transfer from the image section to the register is into the phase 1 and 2 electrodes, i.e. E/F1, G/H1, E/F2 and G/H2. These electrodes must be held at clock “high” level during the process. If the register pulses are designated RØ1, RØ2 and RØ3, then connections should be made as tabulated below.

Clock Generator Drive Pulse Name	RØ1	RØ2	RØ3
E section	E1/F1	E2/F2	E3/F3
G section	G1/H1	G2/H2	G3/H3

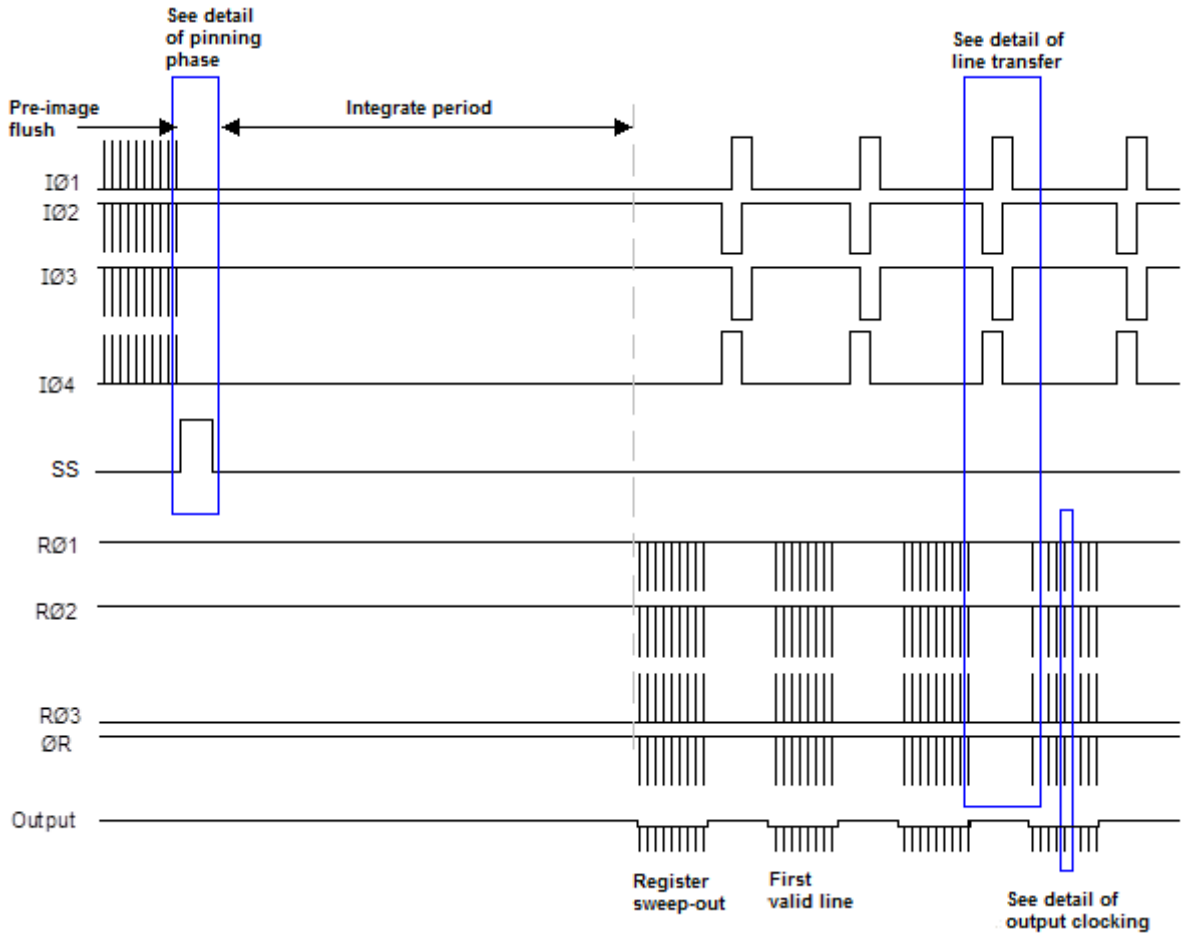
The last electrode before the output gate is separately connected to give the function of a summing well (SW). In normal readout (i.e. if not used for summing), SW is clocked as RØ3. For summing, the selected SW gate is held at clock “high” level for the required number of readout cycles, and then clocked as RØ3 to output charge.

Alternatively, SW may be operated as a second output gate to provide the option of operation in low gain/high signal mode (mode 2) with OG high. If this mode of operation is used, then the sequencing of the output clocks must be changed, as charge now transfers into the output node as RØ2 goes low (see note 9 above also).

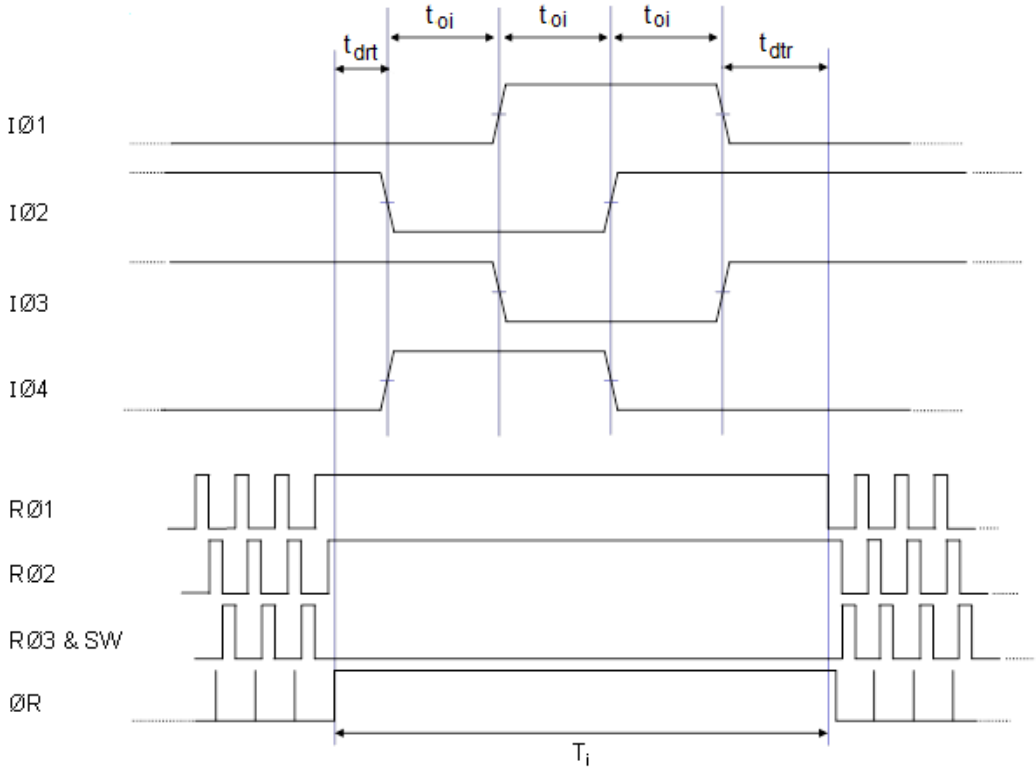
Image phases 2 and 3 should be held high during signal collection, as shown in the following figures.

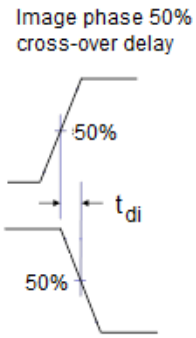
The register is provided with an anti-blooming dump drain to limit the peak signal capacity. For charge dumping purposes rows of charge signals may be clocked into the register sections and any excess charge above full-well capacity spills into the drain. There must then be a single line read-out to remove the unwanted charge (i.e. which can be up to the full-well capacity) before transferring the wanted row or rows of charge signals into the register sections. However, please see note 13 above also.

FRAME READ-OUT TIMING DIAGRAM

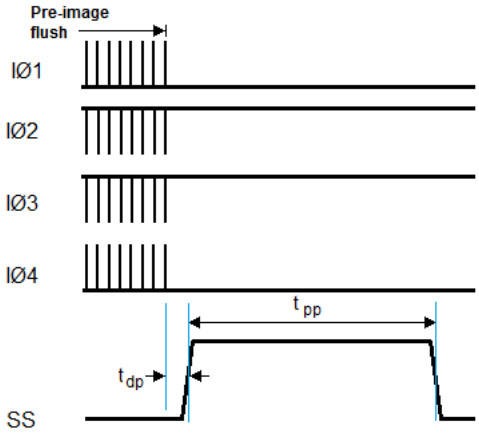


DETAIL OF LINE TRANSFER

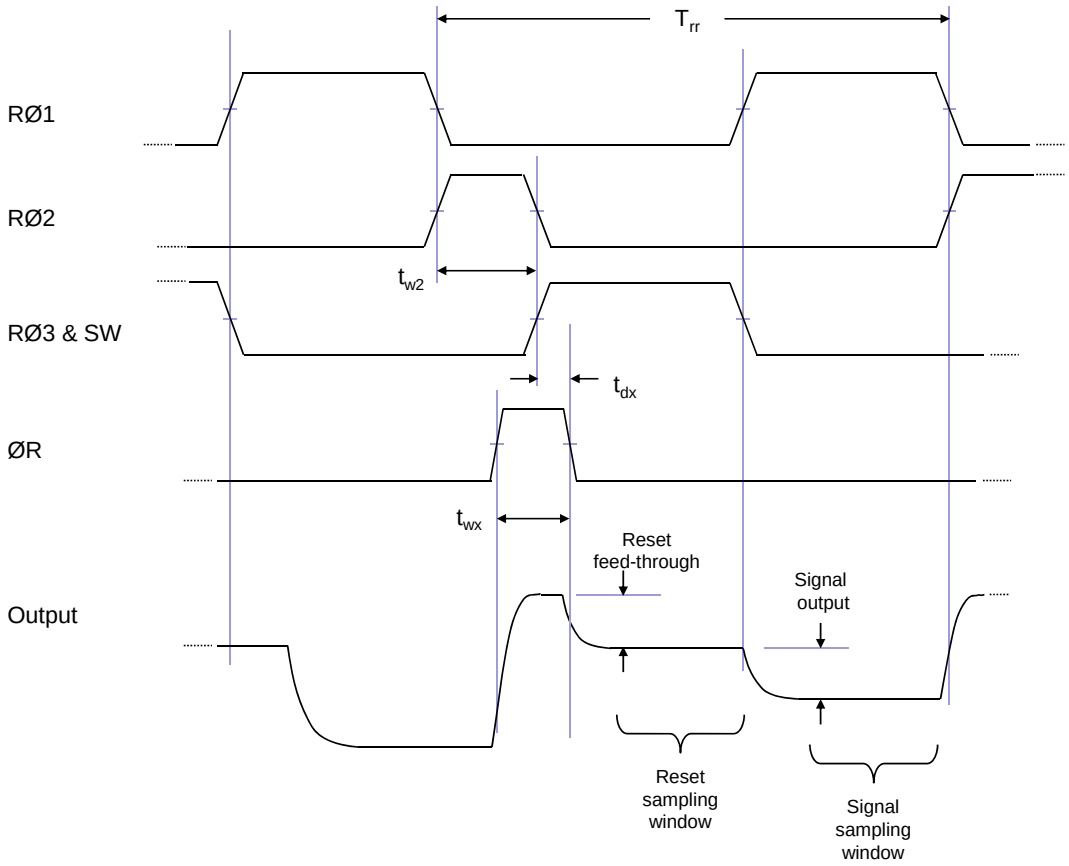


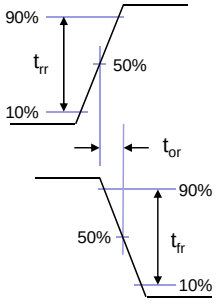


DETAIL OF PINNING PHASE (see note 19)

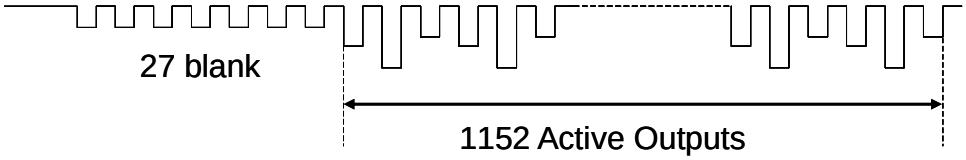


DETAIL OF REGISTER AND OUTPUT CLOCKING (with SW clocked as RØ3)





LINE OUTPUT FORMAT



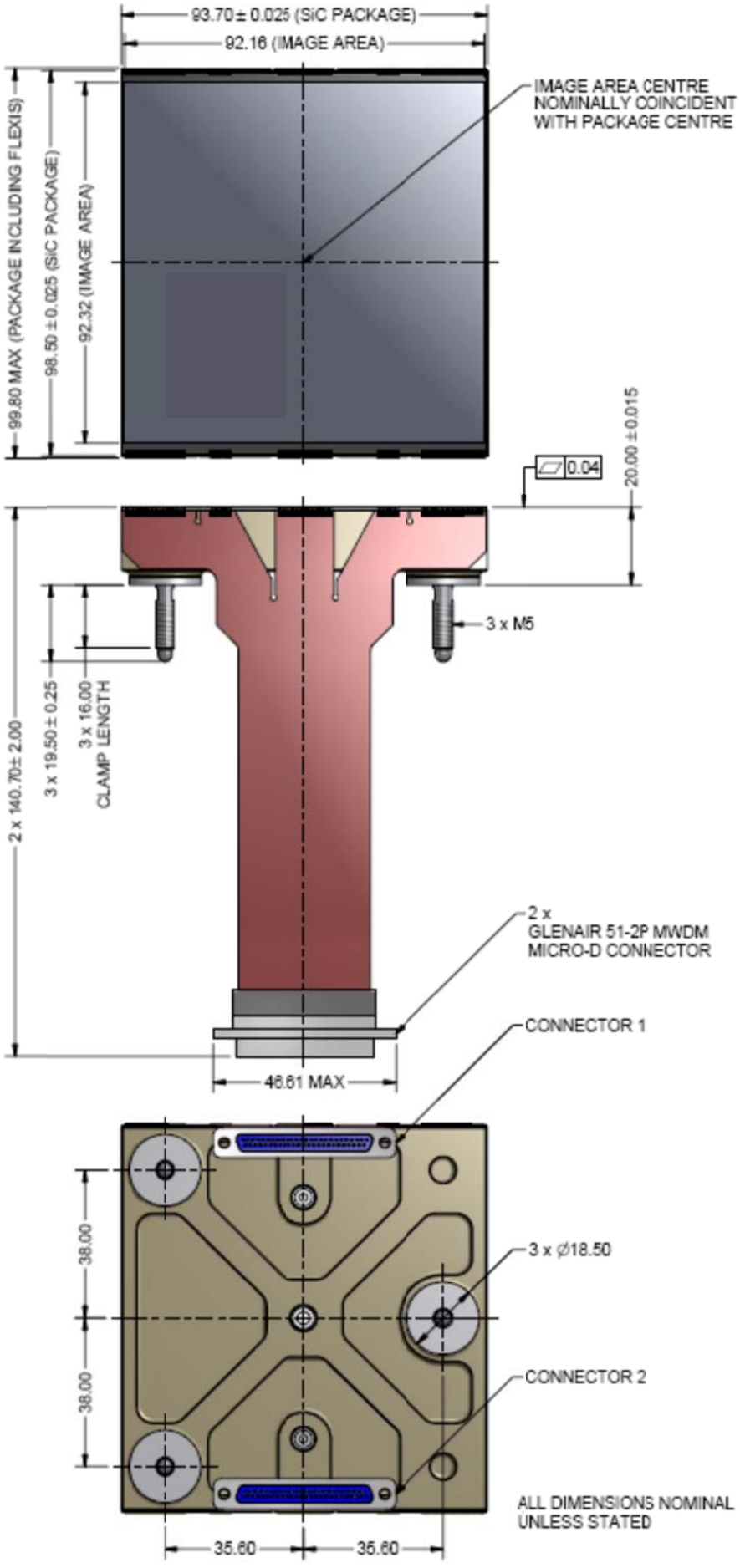
CLOCK TIMING REQUIREMENTS

Symbol	Description	Minimum	Typical	Maximum	Units
T_i	Line transfer time (see note 14)	120	300	-	µs
t_{di}	Delay in falling image clock 50 % point from rising image clock 50 %point (see note 15)	0	30	500	ns
t_{oi}	Image clock pulse overlap	25	60	-	µs
t_{ri}	Image clock and transfer gate pulse rise time	2	5	0.3 t_{oi}	µs
t_{fi}	Image clock and transfer gate pulse fall time	2	5	0.3 t_{oi}	µs
t_{drt}	Delay time, RØ stop to IØ rising	15	30	-	µs
t_{dtr}	Delay time, IØ falling to RØ start	30	80	-	µs
t_{pp}	Substrate high duration during pinning phase	150	150	-	ms
t_{dp}	Delay time, last image clock transition during flush to substrate rising	50	270	500	ms
T_{rr}	Register clock period (see note 16)	300	2000	(see note 17)	ns
t_{w2}	RØ2 pulse width at 50% levels (see note 18)	$3t_{rx}$	350	$T_{rr}/3$	ns
t_{rr}	Register clock pulse rise time	10	70	$0.05T_{rr}$	ns
t_{fr}	Register clock pulse fall time	10	70	$0.05T_{rr}$	ns
t_{or}	Register clock pulse edge overlap at 50% levels	0	50	$0.05T_{rr}$	ns
t_{wx}	Reset pulse width at 50% levels	$3t_{rx}$	300	$0.2T_{rr}$	ns
t_{rx}	Reset pulse rise time	10	50	$0.2t_{wx}$	ns
t_{fx}	Reset pulse fall time	10	50	$0.2t_{wx}$	ns
t_{dx}	Delay time, RØ falling to ØR falling	$2t_{fr}$	150	-	ns

NOTES

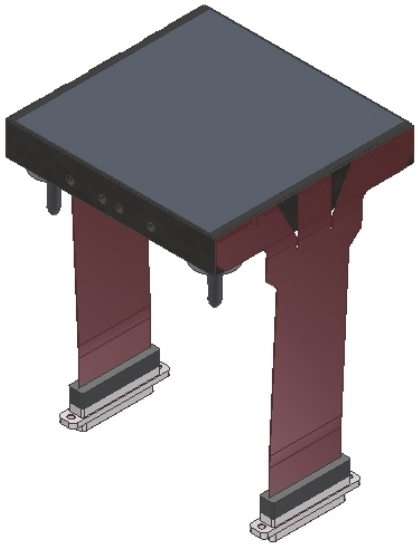
14. $T_i = t_{drt} + 3t_{oi} + t_{dtr}$.
15. The IØ1/IØ3, IØ2/IØ4, IØ3/IØ1 and IØ4/IØ2 transitions are nominally coincident with the edges overlapping at 50% amplitude.
16. The typical timing is for readout at frequencies in the region of 500 kHz, as used for factory tests.
17. For highest speed operation the output load resistor can be reduced from 5 kΩ to approximately 2.2 kΩ, but note that this will increase power consumption. If the device is to be operated with a register clock period of below about 1 MHz, then the load may be increased to 10 kΩ to reduce power consumption.
18. The RØ2 pulse-width is normally minimised, as shown, such that the RØ1 and RØ3 pulse widths can be increased to maximise the output reset and signal sampling intervals.
19. The large area and small pixel size of the CCD290 requires changes to be made to the standard mode of operation, particularly for devices manufactured from deep depletion silicon. This is because for this version of the CCD290, holes are not efficiently removed from the device with standard clocking and it is possible that the structure can be left with holes partially filling the isolation regions giving a photo-response non uniformity along each column. Visually this appears as a “tear” in the image. This effect is most visible with flat field images and is independent of image intensity. To remove this effect the substrate should be pulsed high by +10 V with respect to image clock low for a short period prior to integration, This substrate high pinning phase is implemented by e2v during acceptance testing. Alternatively, the image clocks can be reduced -10V below substrate if independent control of substrate voltage is not available.

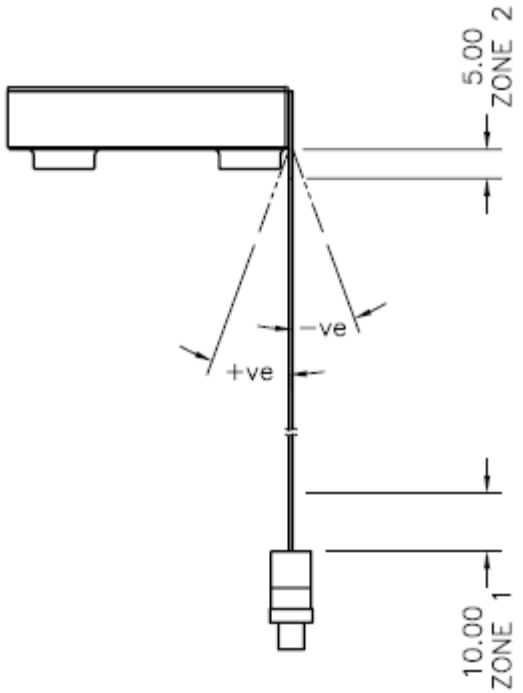
PACKAGE DETAIL



The package base is Silicon Carbide; fitted with two flex-cable connectors and three mounting studs.

Interface drawing DAS772494AT (available on request) provides further information





The bend radius of the flexi PCB is recommended to be no less than 10 mm, with an absolute minimum of 5.8 mm. There should be no forced bending within 10mm of the connector potting (zone 1). There should be no forced bending of the flexi in the negative direction within 5 mm of the flexi to package bondline (zone 2).

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases, a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving sockets to be positively grounded

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (i.e. all CCD pins except SS, DD, RD, OD and OS) but not to the other pins.

The devices are assembled in a clean room environment. e2v technologies recommend that similar precautions are taken to avoid contaminating the active surface.

Buttable flex-cable devices require careful handling to avoid damage to silicon, bond wires of flex cables. Avoid stress on flex cables, and contact factory for advice if needed.

HIGH ENERGY RADIATION

Performance parameters will begin to change if the device is subject to ionising radiation. Characterisation data is held at e2v technologies with whom it is recommended that contact be made if devices are to be operated in any high radiation environment.

TEMPERATURE RANGE

Operating temperature range 153 - 323 K

Storage temperature range 148 - 358 K

Performance parameters are measured with the device at a temperature of 173 K and, as a result, full performance is only guaranteed at this nominal operating temperature.

Operation or storage in humid conditions before the sensor taken to low ambient temperatures may give rise to ice on the surface, thereby causing irreversible damage.

Maximum rate of heating or cooling: 5 K/min.

CCD47-20 NIMO Back Illuminated
High Performance NIMO
Back Illuminated CCD Sensor

FEATURES

- 1024 by 1024 1:1 image format
- Image area 13.3 x13.3 mm
- Back Illuminated format
- Frame transfer operation
- 13 μm square pixels
- Symmetrical anti-static gate protection
- Very low noise output amplifiers
- Gated dump drain on output register
- 100% active area

APPLICATIONS

- Spectroscopy
- Scientific Imaging
- Star Tracking
- Medical Imaging

INTRODUCTION

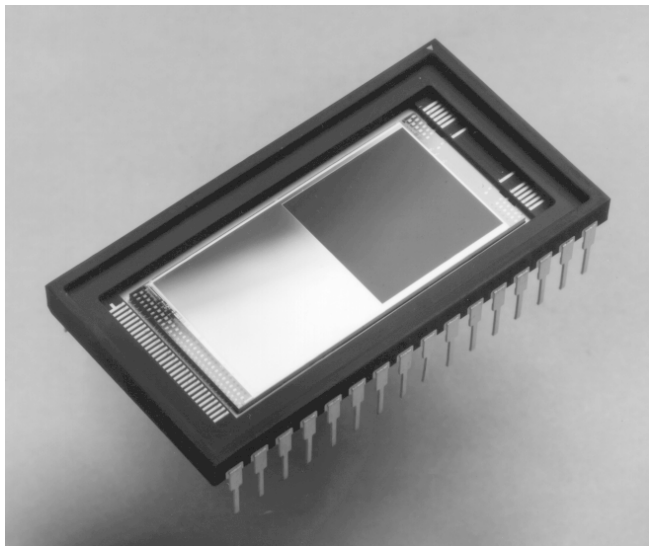
This version of the CCD47 family of CCD sensors has full-frame or frame transfer architecture. Back illumination technology, in combination with extremely low noise amplifiers, makes the device well suited to the most demanding scientific applications. To improve the sensitivity further, the CCD is manufactured without anti-blooming structures.

This device has a single serial output register. Separate charge detection circuits are incorporated at each end of the register, which is split so that a line of charge can be transferred to either output, or split between the two.

The register is provided with a drain and control gate along the outer edge of the channel for charge dump purposes.

Other variants of the CCD47-20 available are front illuminated format and inverted mode. In common with all e2v CCD sensors, the CCD47-20 is also available with a fibre-optic window or taper, or with a phosphor coating.

Designers are advised to consult e2v should they be considering using CCD sensors in abnormal environments or if they require customised packaging.



TYPICAL PERFORMANCE

Maximum readout frequency	5	MHz
Output amplifier responsivity	4.5	μV/e⁻
Peak signal	100	ke⁻/pixel
Dynamic range (at 20 kHz)	≅50,000:1	
Spectral range	200 – 1100	nm
Readout noise (at 20 kHz)	2	e⁻ rms

GENERAL DATA

Format

Image area	13.3 x13.3	mm
Active pixels (H)	1024	
(V)	1024	
Pixel size	13 x 13	μm
Storage area	13.3 x13.3	mm
Pixels (H)	1024	
(V)	1033	

Additional pixels are provided in the image area for dark reference and over-scanning purposes.

Number of output amplifiers	2	
Weight (approx, no window	7.5	g

Package

Package size	22.7 x 42.0	mm
Number of pins	32	
Inter-pin spacing	2.54	mm
Window material	quartz or removable glass	
Package type	ceramic DIL array	

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A1A-100040 Version 3, July 2011
Template: DF764388A-5
110359

PERFORMANCE

	Min	Typical	Max	
Peak charge storage (see note 1)	80k	120k	-	e^-/pixel
Peak output voltage (no binning)	-	540	-	mV
Dark signal at 293 K (see notes 2 and 3)	-	20	40	ke^-/pixel/s
Dynamic range (see note 4)	-	50,000:1	-	
Charge transfer efficiency (see note 5): parallel serial	 - -	 99.9999 99.9993	 - -	 % %
Output amplifier responsivity (see note 3)	3.0	4.5	6.0	$\mu V/e^-$
Readout noise at 253 K (see notes 3 and 6)	-	2.0	4.0	rms e^-/pixel
Maximum readout frequency (see note 7)	-	5.0	-	MHz
Dark signal non-uniformity at 293 K (std. deviation) (see notes 3 and 8)	-	2	4	ke^-/pixel/s

Note: Register capacity is 4x the image peak charge storage.

SPECTRAL RESPONSE AT 253 K

Wavelength (nm)	Minimum Response (QE)			Maximum Response Non-uniformity (1σ)	
	Midband Coated	Broadband Coated	Uncoated		
300	not specified	not specified	not specified	-	%
350	15	25	10	5	%
400	40	55	25	3	%
500	85	75	55	3	%
650	85	75	50	3	%
900	30	30	30	5	%

ELECTRICAL INTERFACE CHARACTERISTICS

Electrode Capacitances (Measured at mid-clock level)

	Min	Typical	Max	
S∅/S∅ interphase	-	3.5	-	nF
I∅/I∅ interphase	-	3.5	-	nF
I∅/SS and S∅/SS	-	4.5	-	nF
R∅/R∅ interphase	-	40	-	pF
R∅/(SS + DG + OD)	-	60	-	pF
∅R/SS	-	10	-	pF
Output impedance at typical operating conditions	-	300	-	Ω

NOTES

1. Signal level at which resolution begins to degrade.
2. Measured between 243 and 293 and V_{SS} +9.5 V. The typical average (background) dark signal at any temperature T (kelvin) between 230 K and 300 K may be estimated from:

   $$Q_d/Q_{d0} = 122T^3e^{-6400/T}$$

   where Q_{d0} is the dark signal at 293 K.
3. Test carried out at e2v on all sensors.
4. Dynamic range is the ratio of full-well capacity to readout noise measured at 243 K and 20 kHz readout frequency.
5. CCD characterisation measurements made using charge generated by X-ray photons of known energy.
6. Measured using a dual-slope integrator technique (i.e. correlated double sampling) with a 20 μs integration period.
7. Readout at speeds in excess of 5 MHz into a 15 pF load can be achieved but performance to the parameters given cannot be guaranteed.
8. Measured between 243 and 293 K, excluding white defects.

BLEMISH SPECIFICATION

Traps Pixels where charge is temporarily held. Traps are counted if they have a capacity greater than 200 e^- at 243 K.

Slipped columns Are counted if they have an amplitude greater than 200 e^-.

Black spots Are counted when they have a signal level of less than 80% of the local mean at a signal level of approximately half full-well.

White spots Are counted when they have a generation rate 25 times the specified maximum dark signal generation rate (measured between 243 and 293 K). The typical temperature dependence of white spot blemishes is the same as that of the average dark signal i.e.:

$$Q_d/Q_{d0} = 122T^3e^{-6400/T}$$

White column A column which contains at least 21 white defects.

Black column A column which contains at least 21 black defects.

GRADE	0	1	2
Column defects; black or slipped	0	2	6
white	0	0	2
Black spots	50	100	200
Traps >200 e^-	2	5	12
White spots	50	80	100

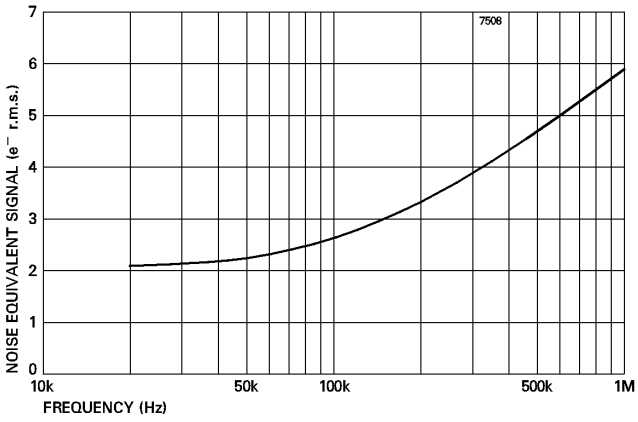
Grade 5 Devices which are fully functional, with image quality below that of grade 2, and which may not meet all other performance parameters.

Note: The effect of temperature on defects is that traps will be observed less at higher temperatures but more may appear below 243 K. The amplitude of white spots and columns will decrease rapidly with temperature.

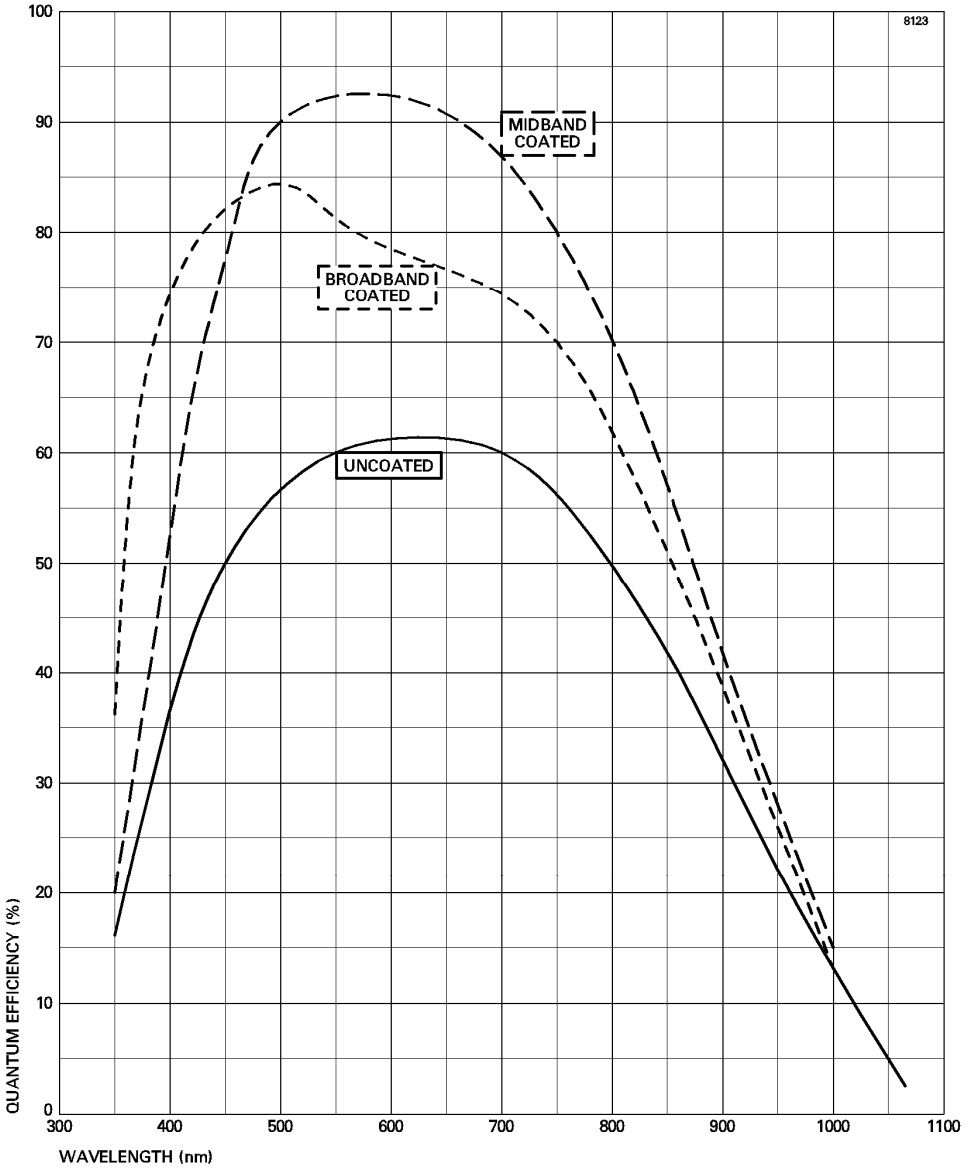
TYPICAL OUTPUT CIRCUIT NOISE

(Measured using clamp and sample)

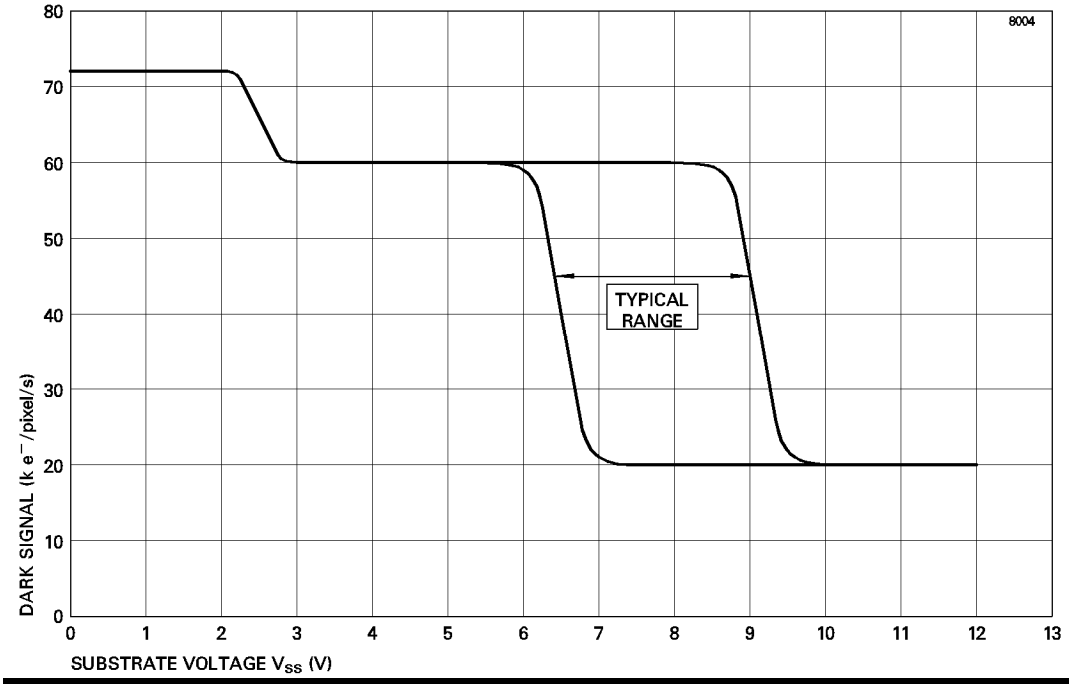
V_{SS} = 9.5 V, V_{RD} = 17 V, V_{OD} = 29 V



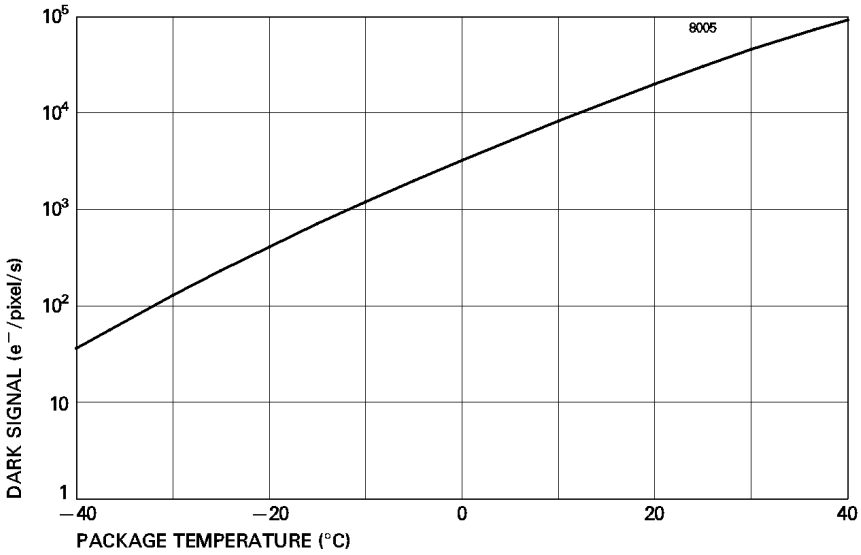
TYPICAL SPECTRAL RESPONSE (At –20 °C, no window)



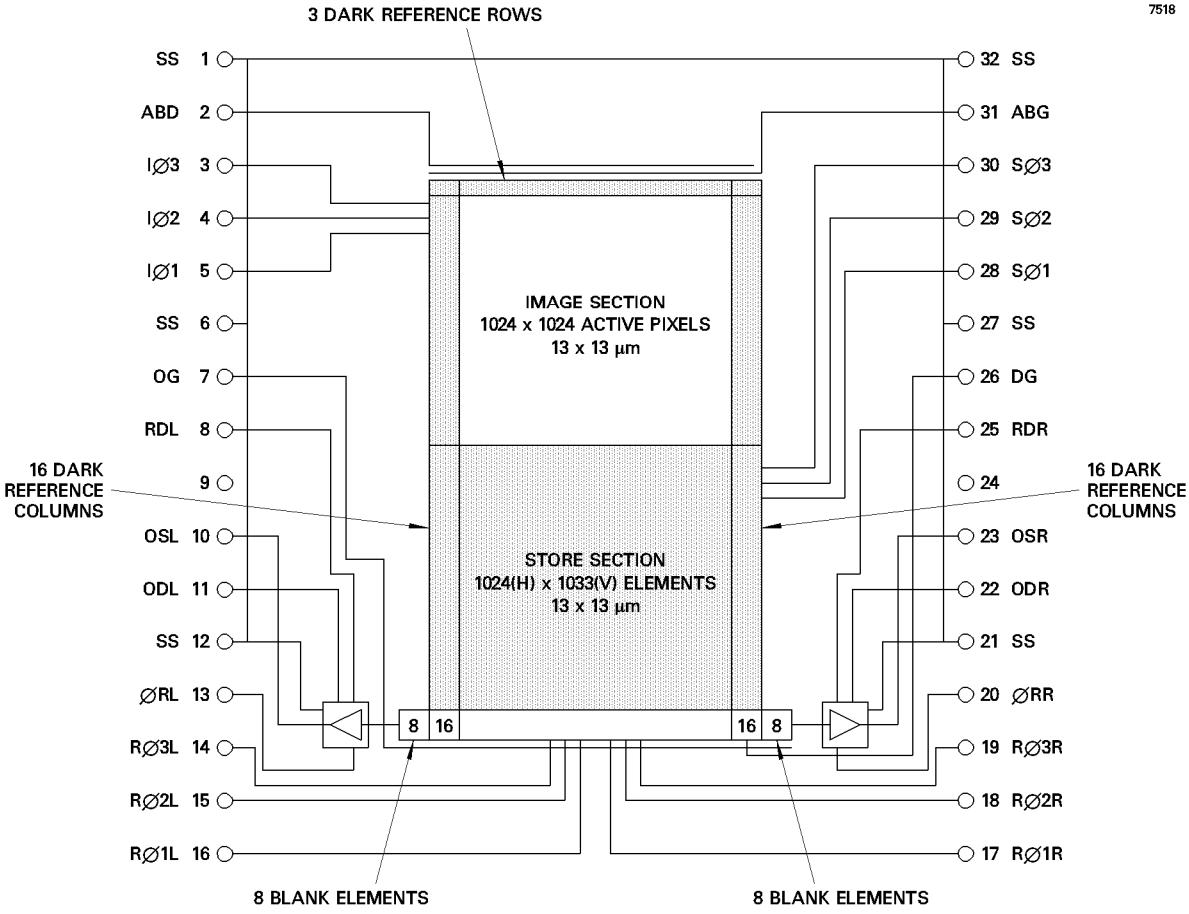
TYPICAL VARIATION OF DARK CURRENT WITH SUBSTRATE VOLTAGE



TYPICAL VARIATION OF DARK SIGNAL WITH TEMPERATURE (V_{SS} = +9.5 V)



DEVICE SCHEMATIC



CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

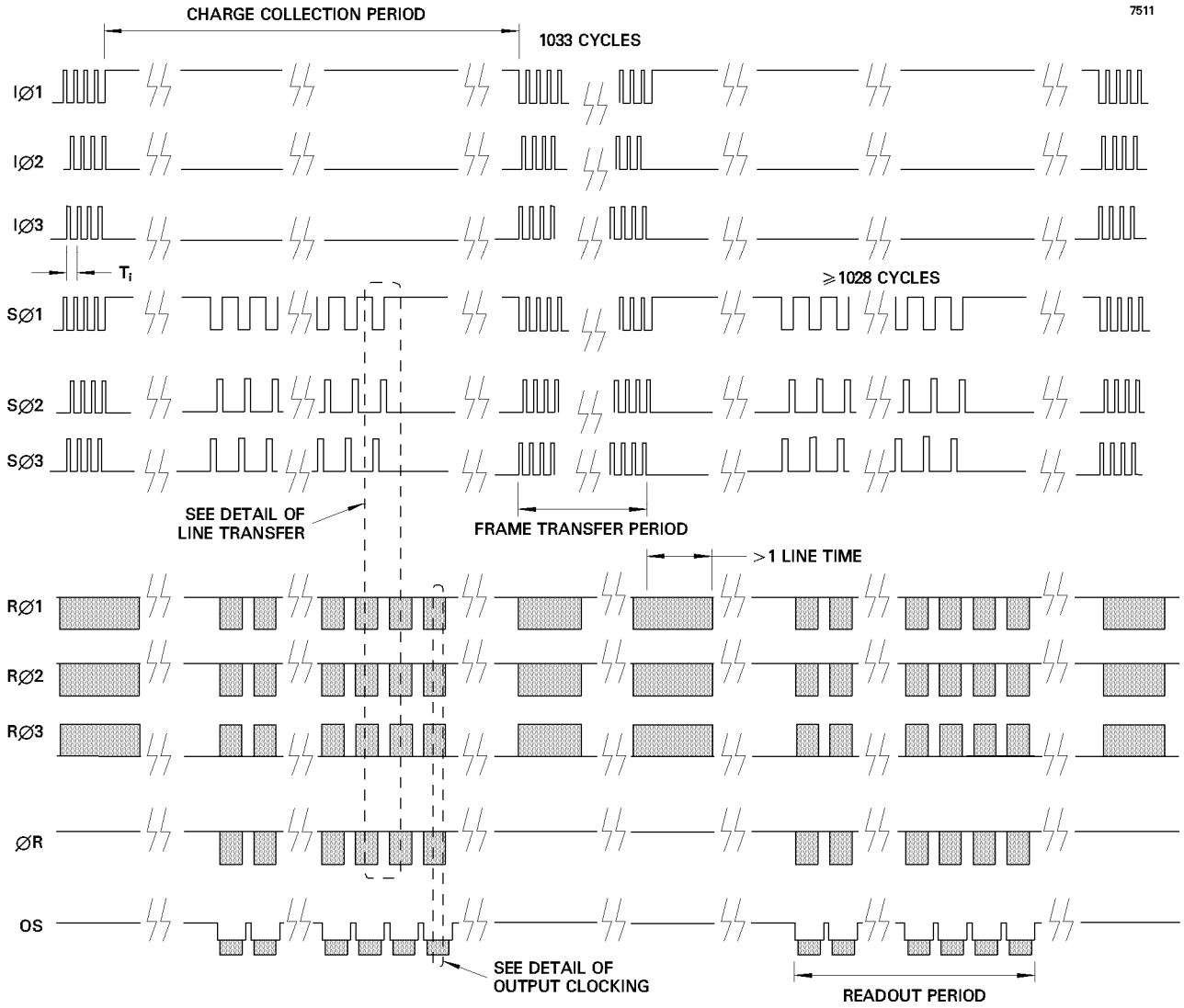
PIN	REF	DESCRIPTION	PULSE AMPLITUDE OR DC LEVEL (V) (See note 9)			MAXIMUM RATINGS with respect to V_{SS}
			Min	Typical	Max	
1	SS	Substrate	0	9	10	-
2	ABD	Anti-blooming drain (see note 10)		V_{OD}		–0.3 to +25 V
3	I∅3	Image area clock, phase 3	8	12	15	±20 V
4	I∅2	Image area clock, phase 2	8	12	15	±20 V
5	I∅1	Image area clock, phase 1	8	12	15	±20 V
6	SS	Substrate	0	9	10	-
7	OG	Output gate	1	3	5	±20 V
8	RDL	Reset transistor drain (left amplifier)	15	17	19	–0.3 to +25 V
9	-	No connection		-		-
10	OSL	Output transistor source (left amplifier)		see note 11		–0.3 to +25 V
11	ODL	Output transistor drain (left amplifier)	27	29	32	–0.3 to +35 V
12	SS	Substrate	0	9	10	-
13	∅RL	Output reset pulse (left amplifier)	8	12	15	±20 V
14	R∅3L	Output register clock phase 3 (left section)	8	10	15	±20 V
15	R∅2L	Output register clock phase 2 (left section)	8	10	15	±20 V
16	R∅1L	Output register clock phase 1 (left section)	8	10	15	±20 V
17	R∅1R	Output register clock phase 1 (right section)	8	10	15	±20 V
18	R∅2R	Output register clock phase 2 (right section)	8	10	15	±20 V
19	R∅3R	Output register clock phase 3 (right section)	8	10	15	±20 V
20	∅RR	Output reset pulse (right amplifier)	8	12	15	±20 V
21	SS	Substrate	0	9	10	-
22	ODR	Output transistor drain (right amplifier)	27	29	32	–0.3 to +35 V
23	OSR	Output transistor source (right amplifier)		see note 11		–0.3 to +25 V
24	-	No connection		-		-
25	RDR	Reset transistor drain (right amplifier)	15	17	19	–0.3 to +25 V
26	DG	Dump gate (see note 12)	-	0	-	±20 V
27	SS	Substrate	0	9	10	-
28	S∅1	Storage area clock, phase 1	8	12	15	±20 V
29	S∅2	Storage area clock, phase 2	8	12	15	±20 V
30	S∅3	Storage area clock, phase 3	8	12	15	±20 V
31	ABG	Anti-blooming gate	0	0	5	±20 V
32	SS	Substrate	0	9	10	-

Maximum voltages between pairs of pins:
pin 10 (OSL) to pin 11 (ODL) ..... +15 V
pin 22 (ODR) to pin 23 (OSR) ..... +15 V
Maximum output transistor current ..... 10 mA

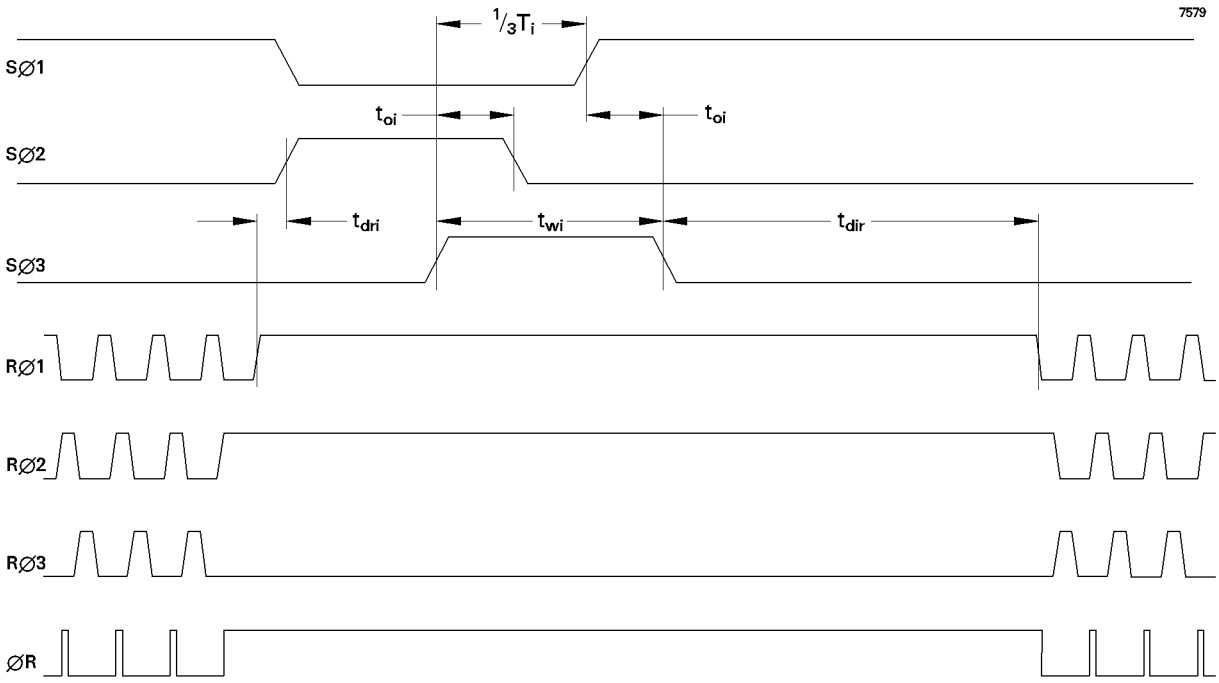
NOTES

9. Readout register clock pulse low levels +1 V; other clock low levels 0 ± 0.5 V.
10. Drain not incorporated, but bias is still necessary.
11. 3 to 5 V below OD. Connect to ground using a 2 to 5 mA current source or appropriate load resistor (typically 5 to 10 kΩ).
12. Non-charge dumping level shown. For operation in charge dumping mode, DG should be pulsed to 12 ± 2 V.
13. All devices will operate at the typical values given. However, some adjustment within the minimum to maximum range may be required to optimise performance for critical applications. It should be noted that conditions for optimum performance may differ from device to device.
14. With the R∅ connections shown, the device will operate through the right-hand output only. In order to operate from both outputs, R∅1(L) and R∅2(L) should be reversed.

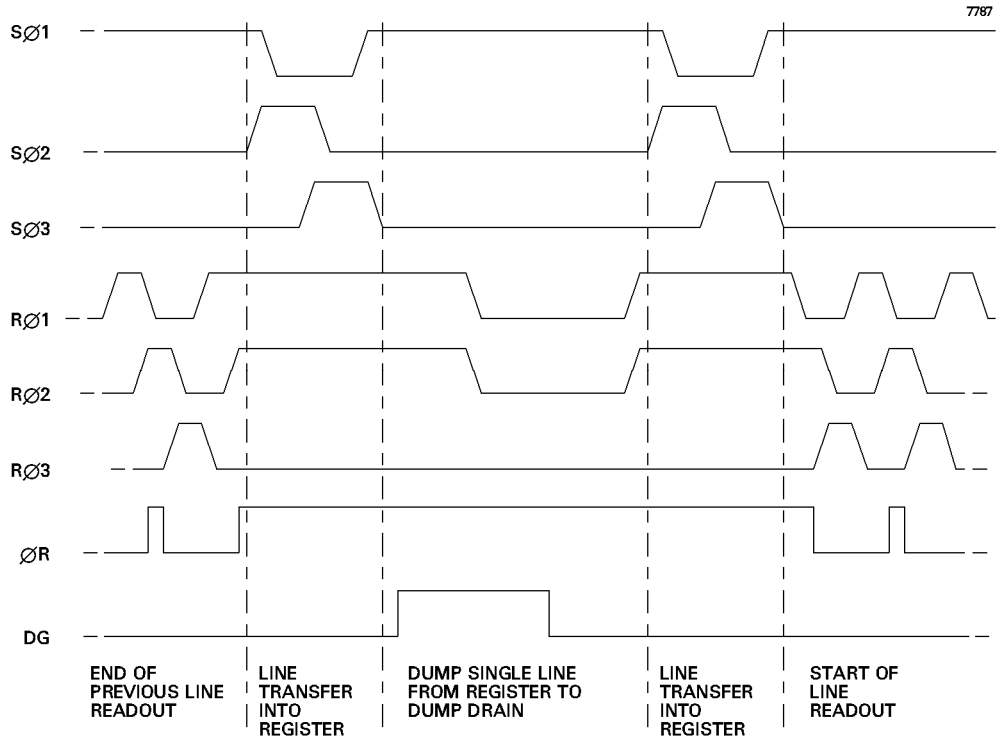
FRAME TRANSFER TIMING DIAGRAM



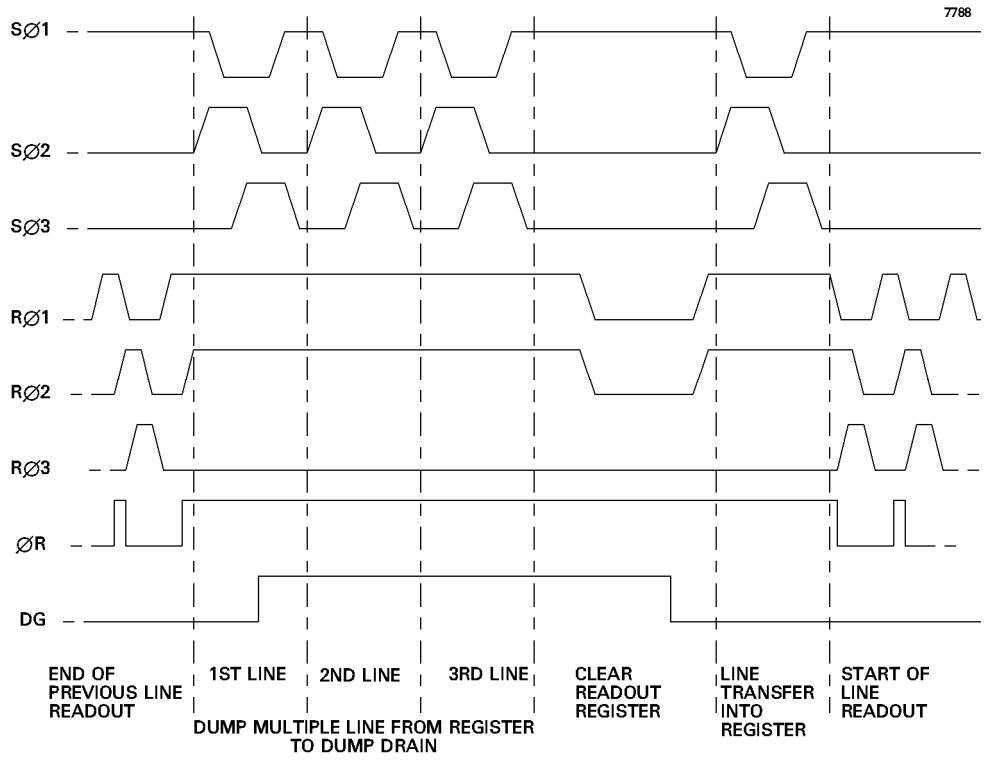
DETAIL OF LINE TRANSFER



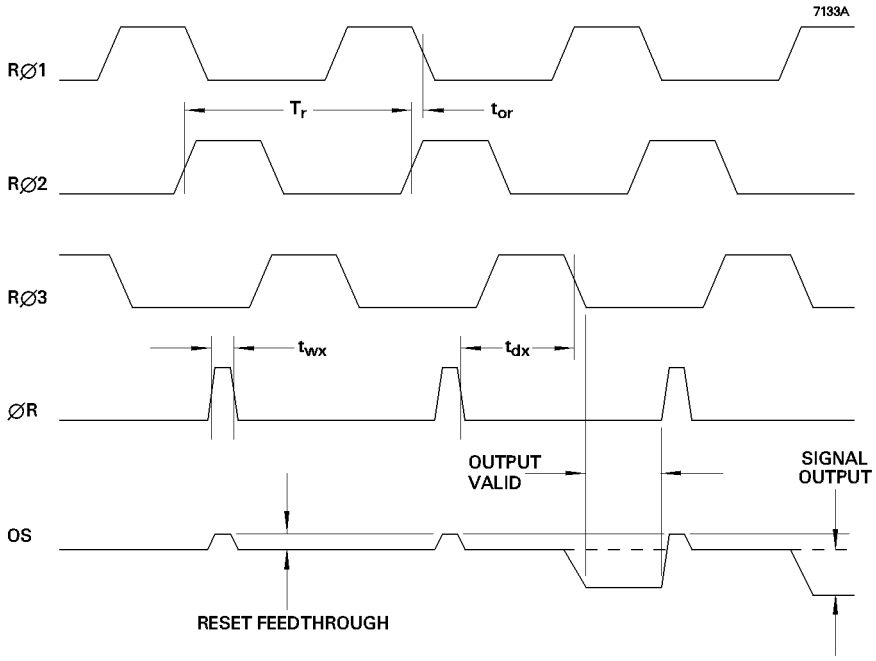
DETAIL OF VERTICAL LINE TRANSFER



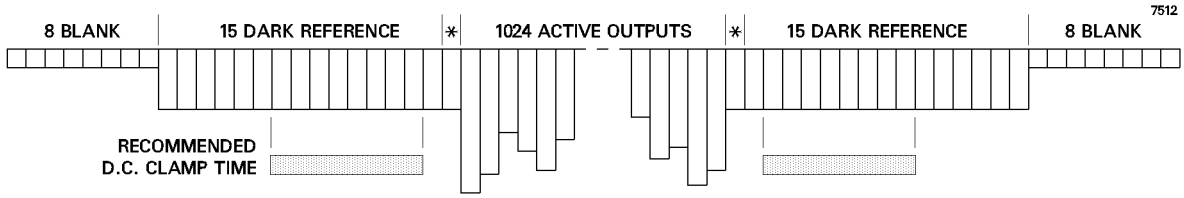
DETAIL OF VERTICAL LINE TRANSFER (Multiple line dump)



DETAIL OF OUTPUT CLOCKING



LINE OUTPUT FORMAT



* = Partially shielded transition elements

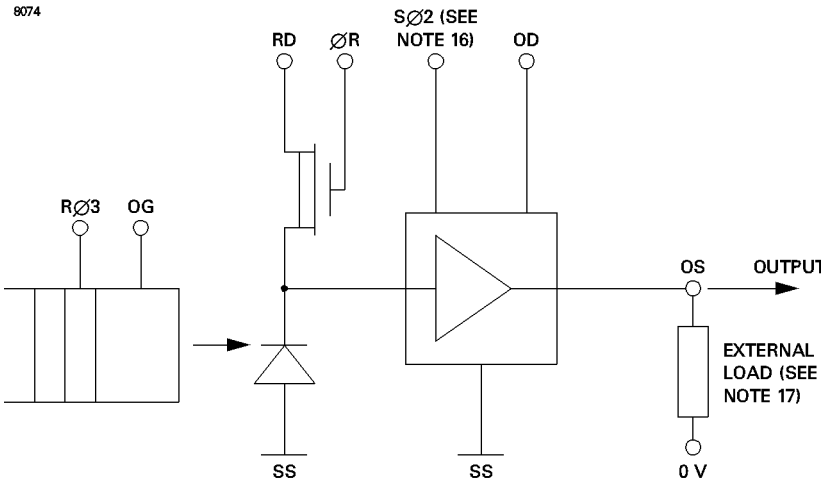
CLOCK TIMING REQUIREMENTS

Symbol	Description	Min	Typical	Max	
T_i	Store clock period	2	5	see note 15	µs
t_{wi}	Image/store clock pulse width	1	2.5	see note 15	µs
t_{ri}	Image/store clock pulse rise time (10 to 90%)	0.1	0.5	$0.2T_i$	µs
t_{fi}	Image/store clock pulse fall time (10 to 90%)	t_{ri}	0.5	$0.2T_i$	µs
t_{oi}	Image/store clock pulse overlap	$(t_{ri} + t_{fi})/2$	0.5	$0.2T_i$	µs
t_{dir}	Delay time, S∅ stop to R∅ start	1	1	see note 15	µs
t_{dri}	Delay time, R∅ stop to S∅ start	1	1	see note 15	µs
T_r	Output register clock cycle period	200	1000	see note 15	ns
t_{rr}	Clock pulse rise time (10 to 90%)	50	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	20	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	30	$0.1T_r$	$0.3T_r$	ns
t_{rx}, t_{fx}	Reset pulse rise and fall times	$0.2t_{wx}$	$0.5t_{rr}$	$0.1T_r$	ns
t_{dx}	Delay time, ∅R low to R∅3 low	30	$0.5T_r$	$0.8T_r$	ns

NOTES

15. No maximum other than that necessary to achieve an acceptable dark signal at the longer readout times.

OUTPUT CIRCUIT

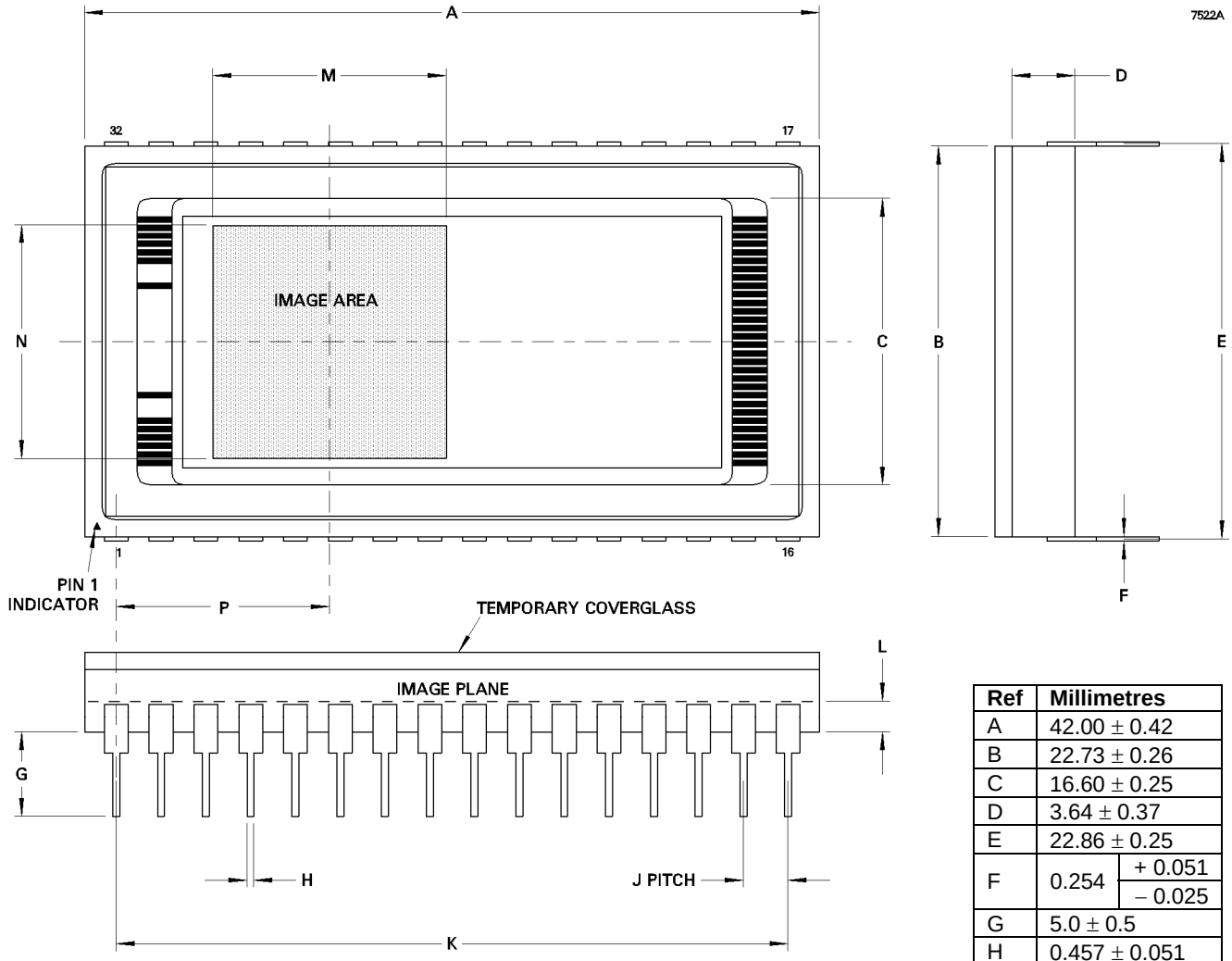


NOTES

16. The amplifier has a DC restoration circuit which is internally activated whenever S∅2 is high.

17. Not critical; can be a 3 to 5 mA constant current supply or an appropriate load resistor.

OUTLINES (All dimensions in millimetres; dimensions without limits are nominal)



Ref	Millimetres
A	42.00 ± 0.42
B	22.73 ± 0.26
C	16.60 ± 0.25
D	3.64 ± 0.37
E	22.86 ± 0.25
F	0.254 +0.051 −0.025
G	5.0 ± 0.5
H	0.457 ± 0.051
J	2.54 ± 0.13
K	38.1
L	1.65 ± 0.25
M	13.3
N	13.3
P	12.2 ± 0.5

ORDERING INFORMATION

Options include:

- Temporary quartz window
- Permanent quartz window
- Temporary glass window
- Permanent glass window
- Fibre-optic coupling
- X-ray phosphor coating

For further information on the performance of these and other options, contact e2v.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty.

HIGH ENERGY RADIATION

Device parameters may begin to change if subject to an ionising dose of greater than 10^4 rads.

Users planning to use CCDs in a high radiation environment are advised to contact e2v.

TEMPERATURE LIMITS

	Min	Typical	Max	
Storage	153	-	373	K
Operating	153	273	323	K

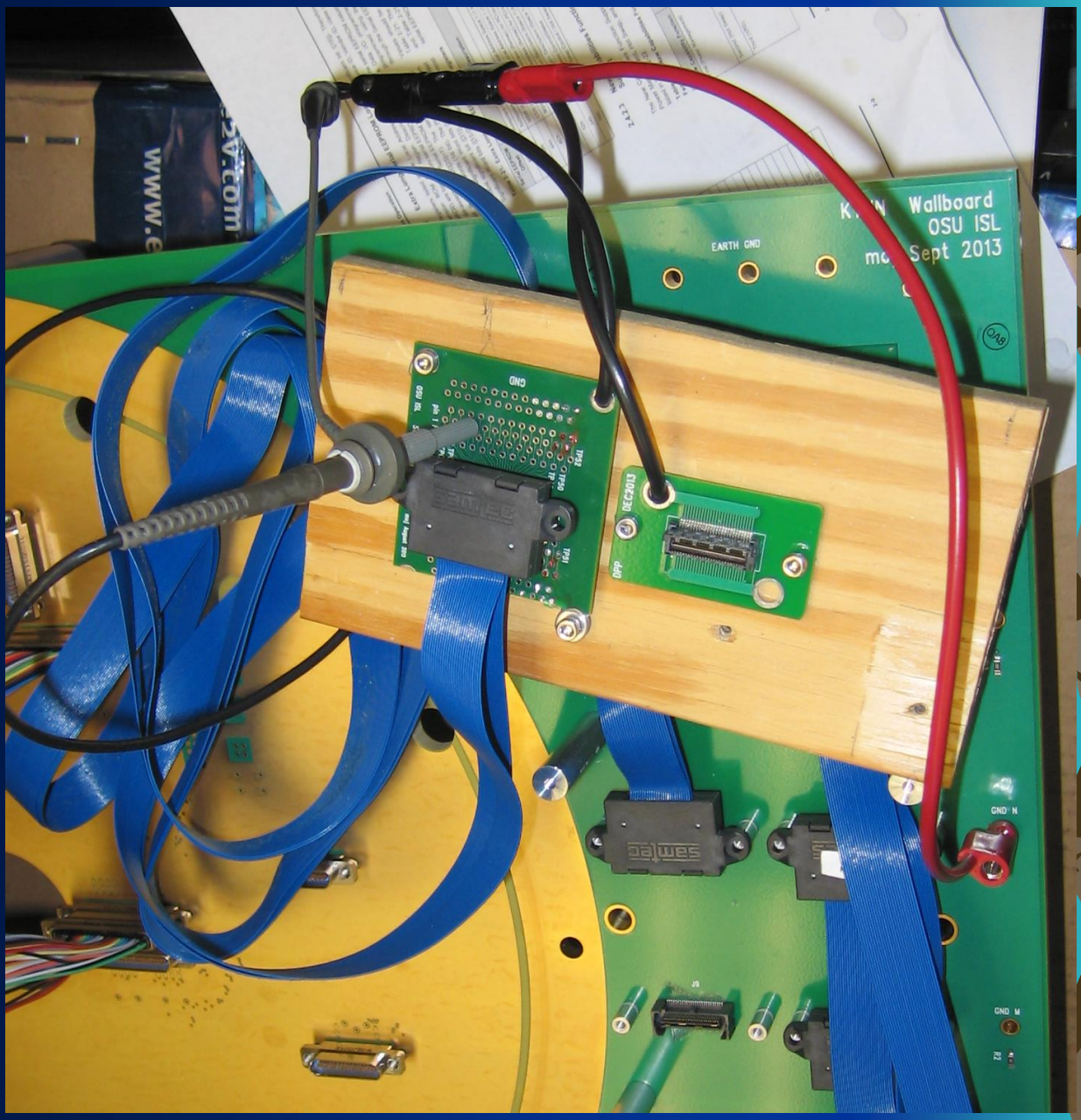
Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling .....5 K/min

KMTN 9K Waveforms

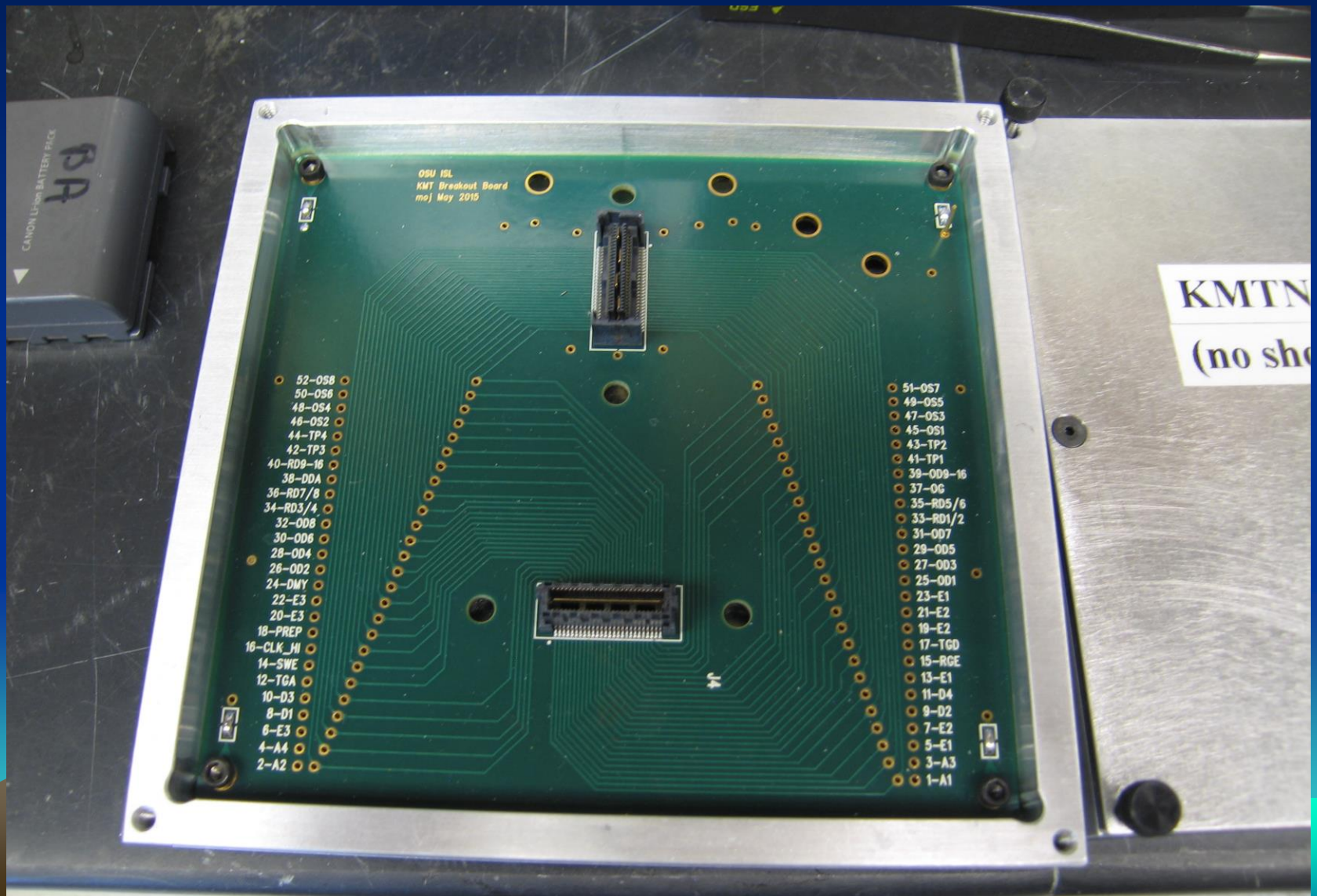
Checking the Clock Signals

Setup, Blue cable between J78 and male breakout board. The picture shows the probe in pin 14 (should have tape on 8 OS pins!)
Note ‘scope probe ground connected to banana plugs


Wallboard
OSU ISL
Sept 2013
EARTH GND
GND
DEC2013
GND N
GND M

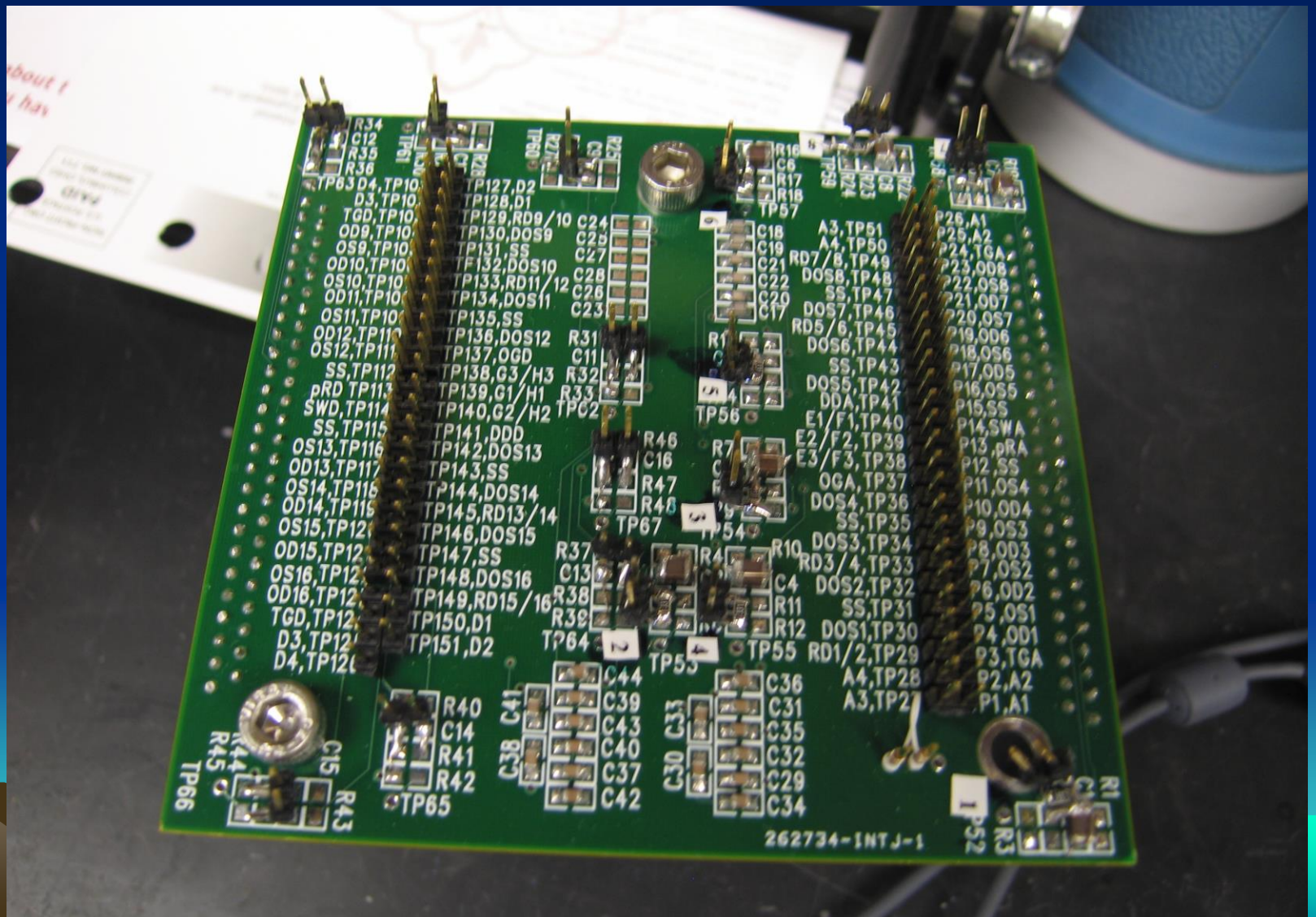
- Better yet, use the new Break-Out Boards in the aluminum boxes. The CCD pin numbers and signal names are labeled

New Break-Out Board

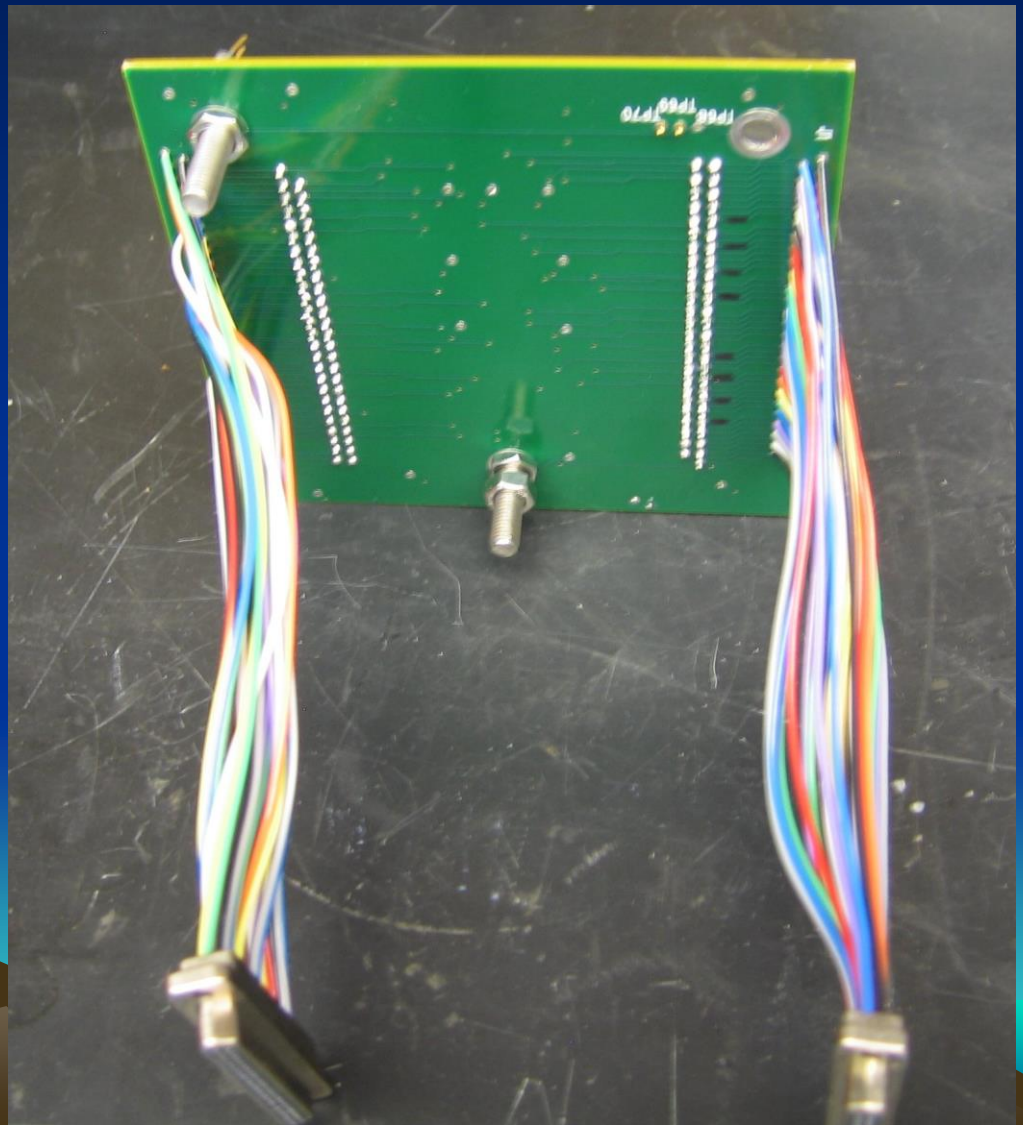


Dummy Load (Top)

(plugs into Wall Board instead of CCD for tests in the lab)



Dummy Load (bottom)



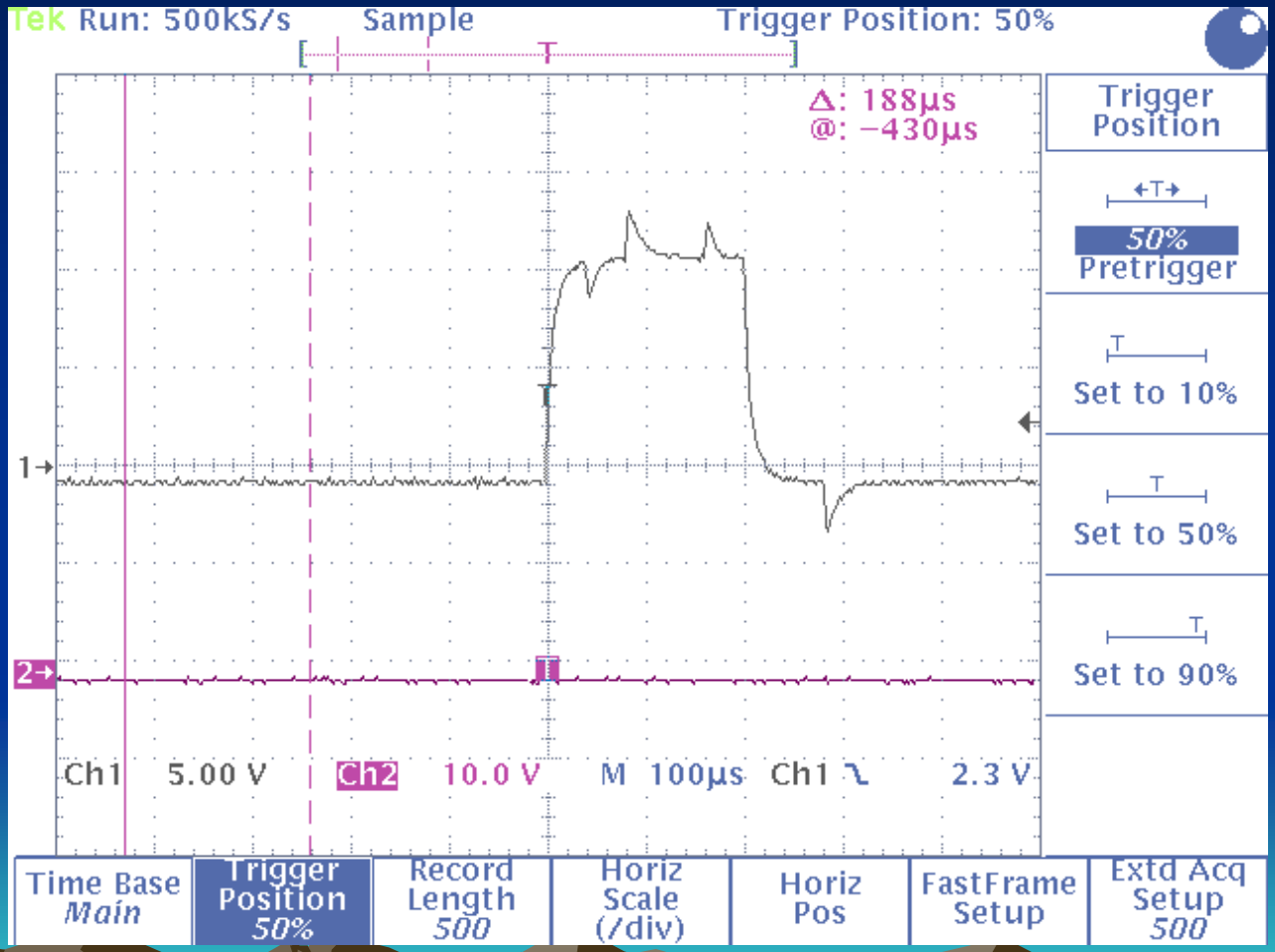
Waveform Notes 1

- All taken with a dummy load, details will be somewhat different when connected to a CCD
- The edges will be sharp and clock-to-clock coupling will be much smaller without the dummy load.
- All waveforms triggered on negative edge and therefore the time relationship between phases is not shown.
- Note that vertical waveforms (A, D and TG) have a time base of 100 microseconds/division while serial waveforms (E, RG and SW) have a timebase of 200 nanoseconds/division.

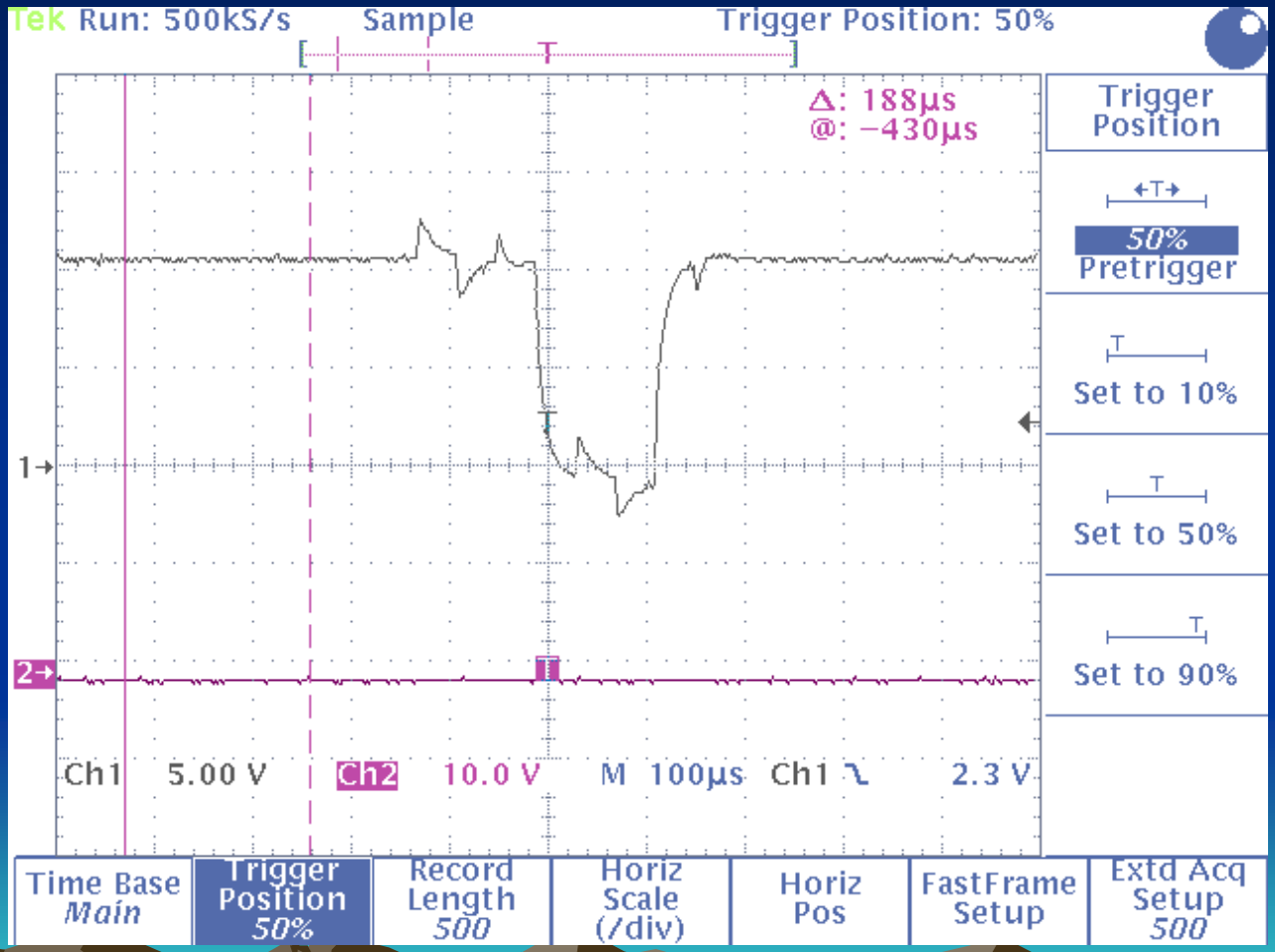
Waveform notes 2

- Note coupling between phases (with dummy load or CCD)
- Note risetime is long for main clock phases (A, D, and E) and short for TG, SW and RG
- Note that each of the E phases is driven by 3 drivers on separate pins

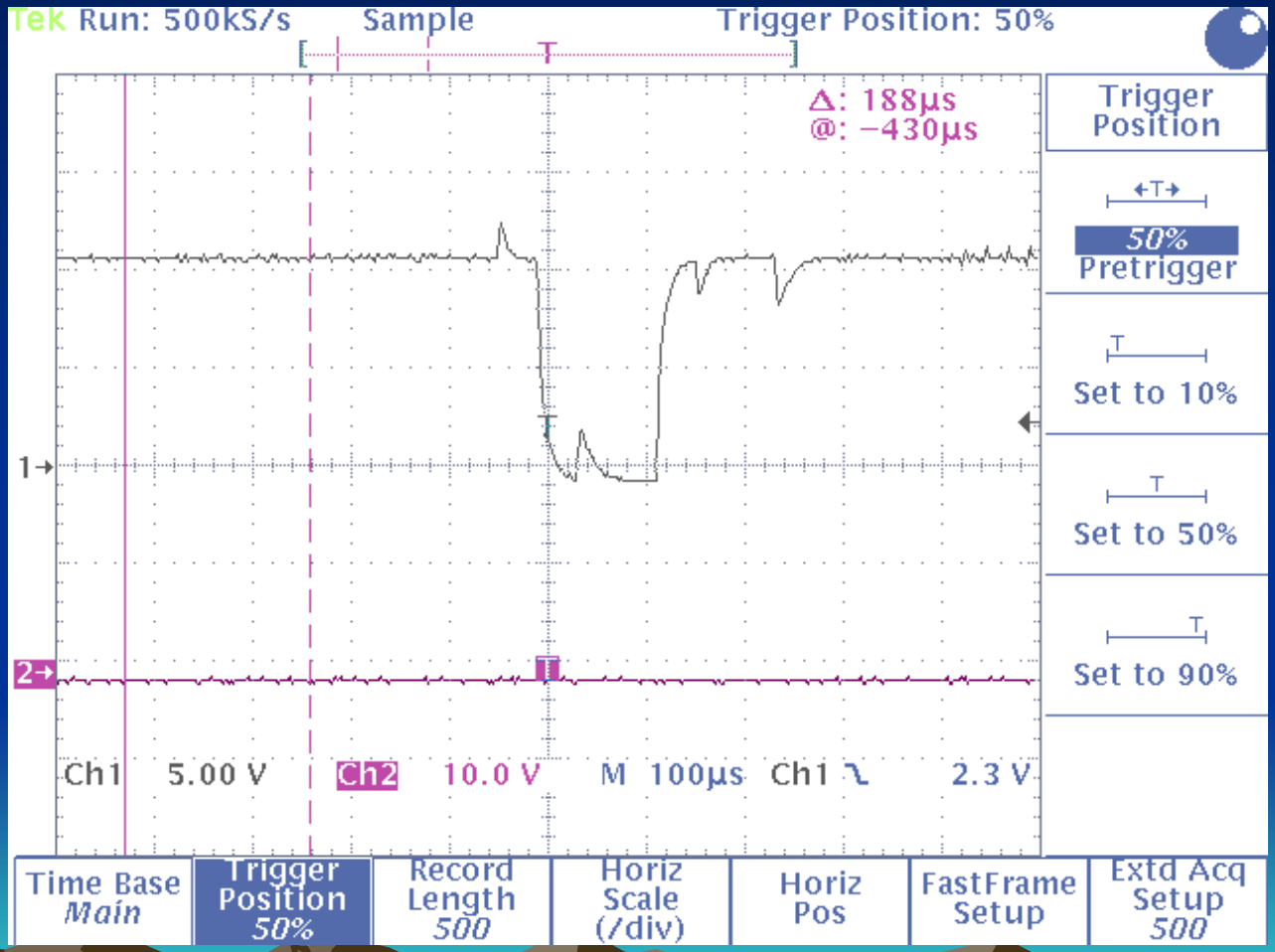
Pin 1 (A phase 1)



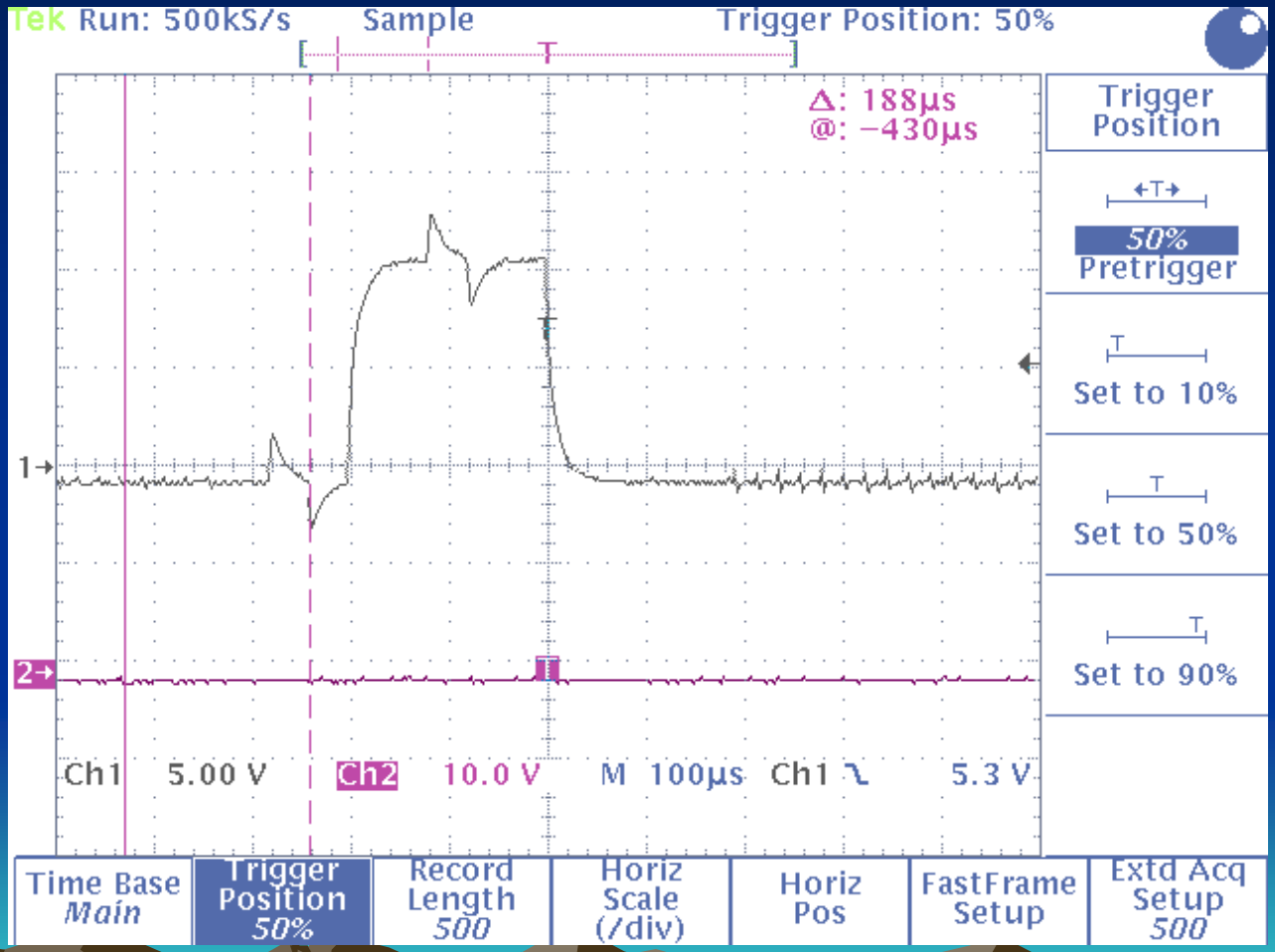
Pin2 (A phase 2)



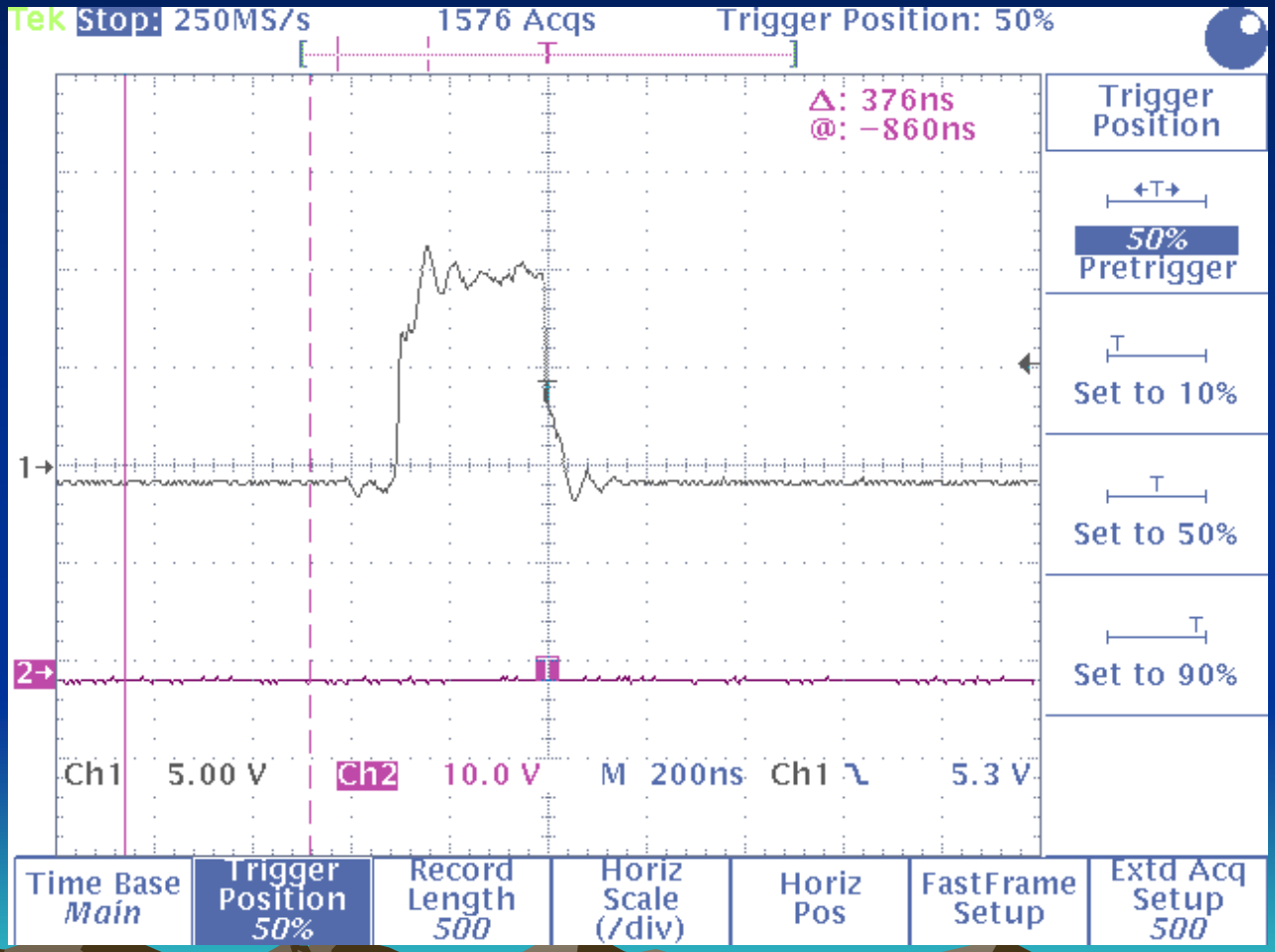
Pin3 (A phase 3)



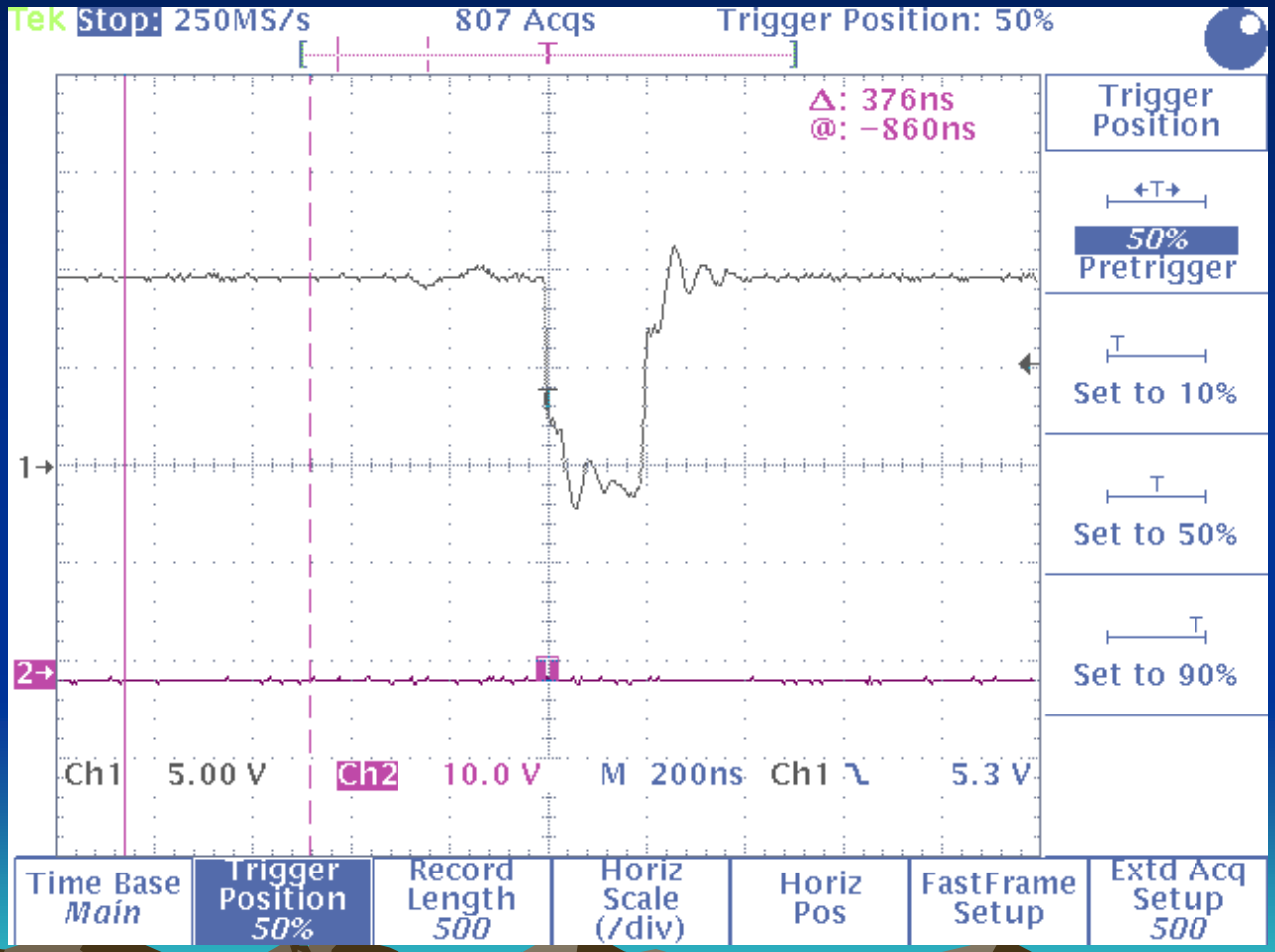
Pin 4 (A phase 4)



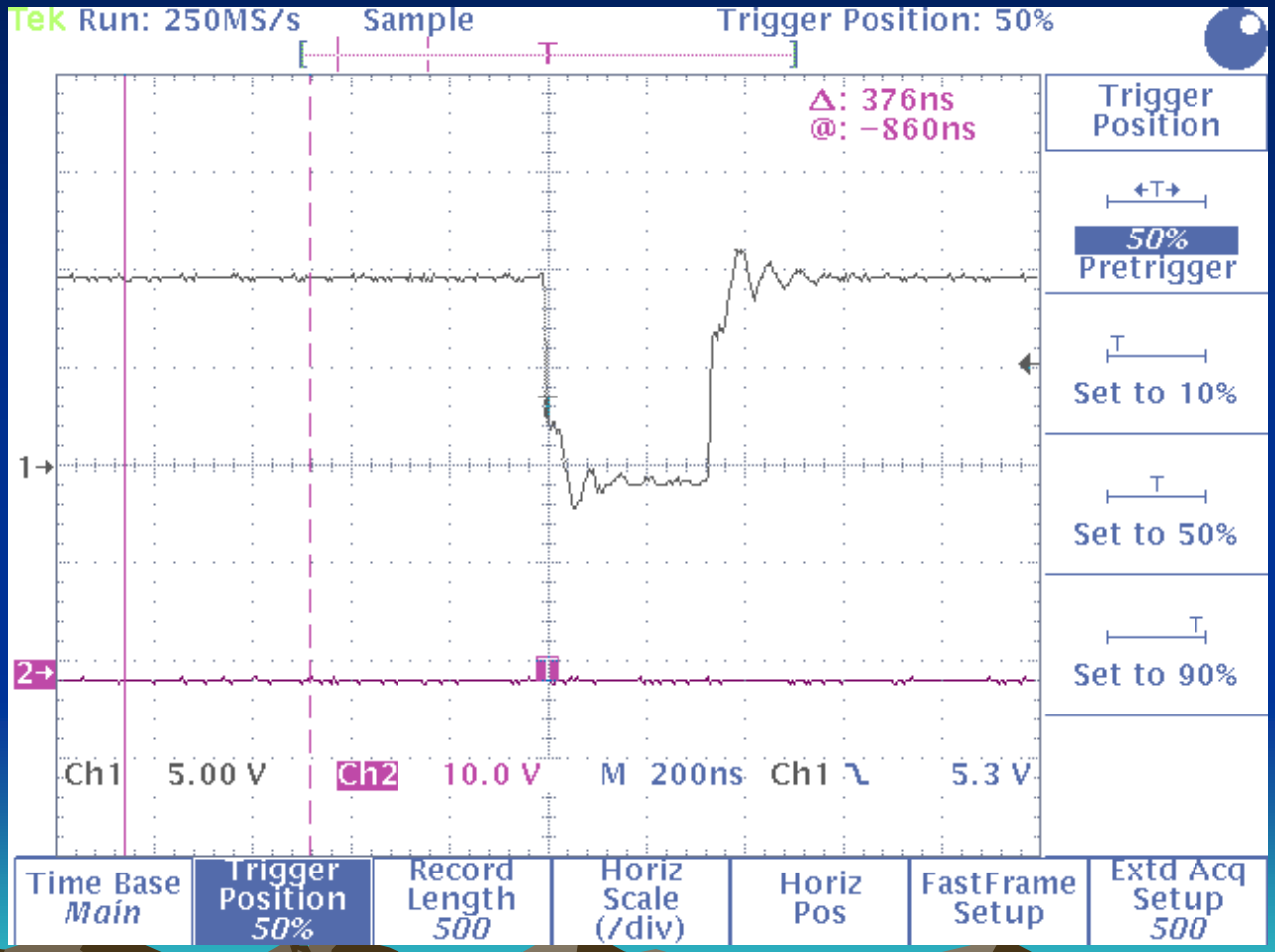
Pin 5 (+ 13 & 23) (E phase 1)



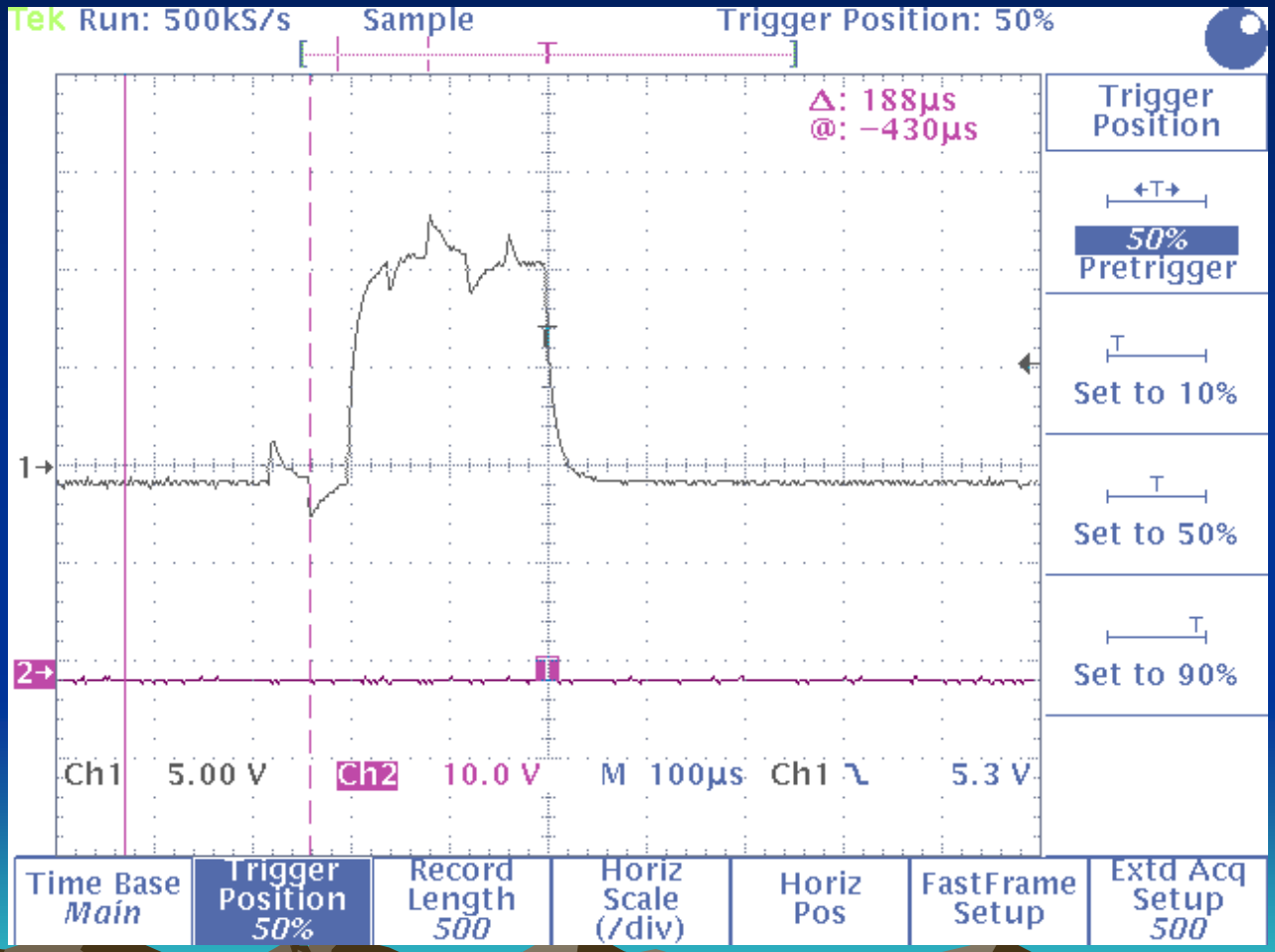
Pin 6 (+20 & 22)(E phase 3)



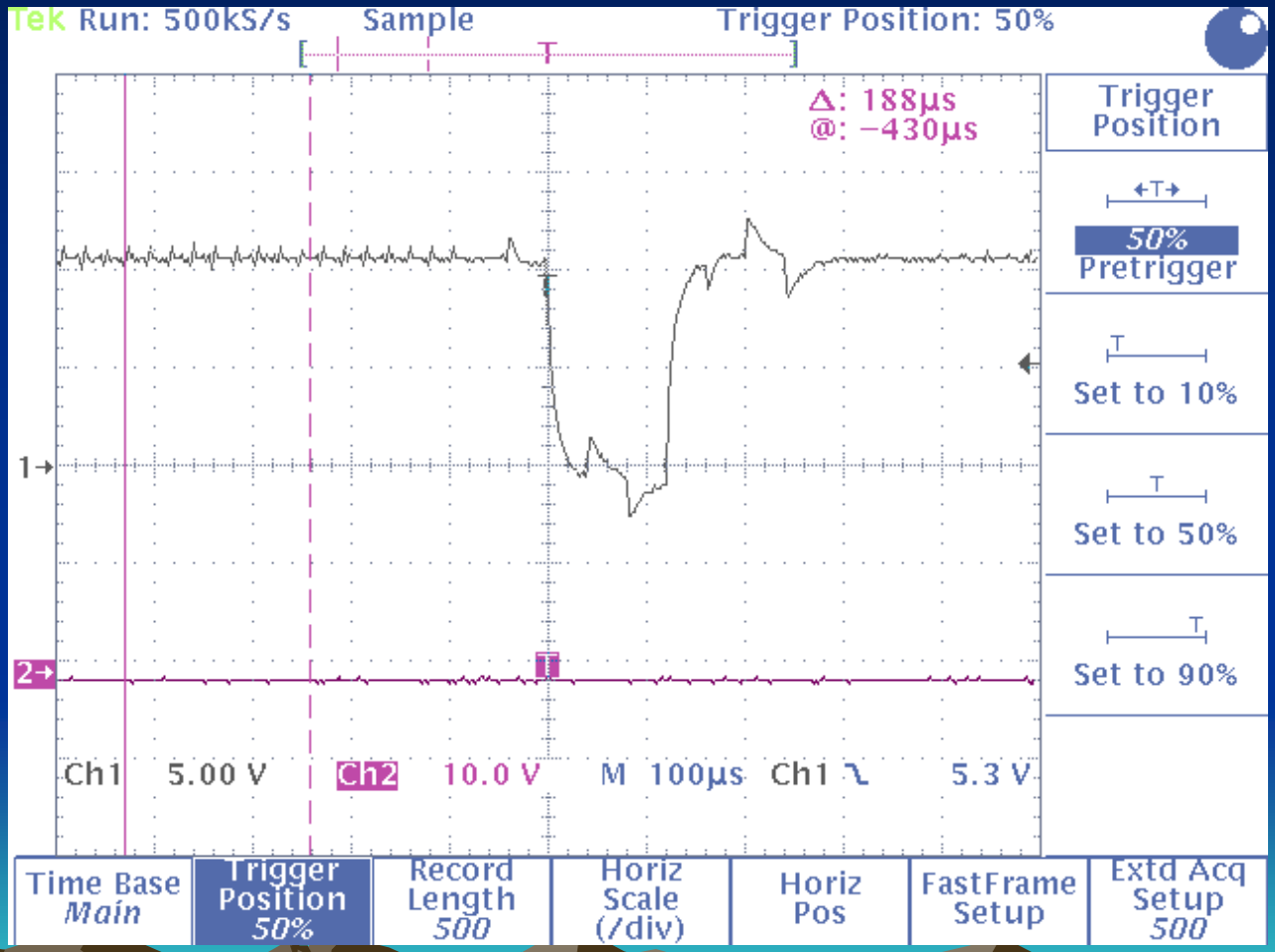
Pin 7 (+19 & 21)(E phase 2)



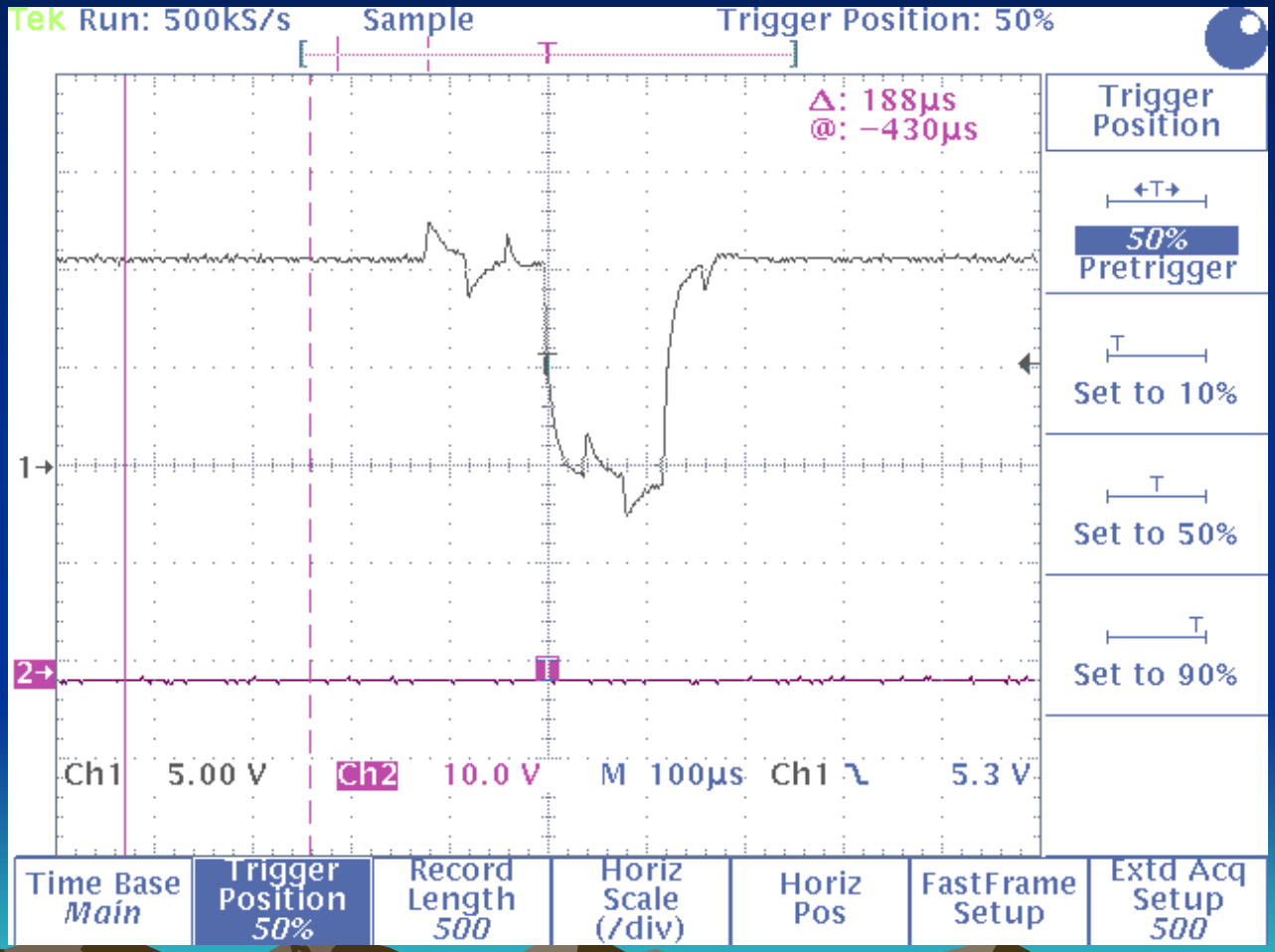
Pin 8 (D phase 1)



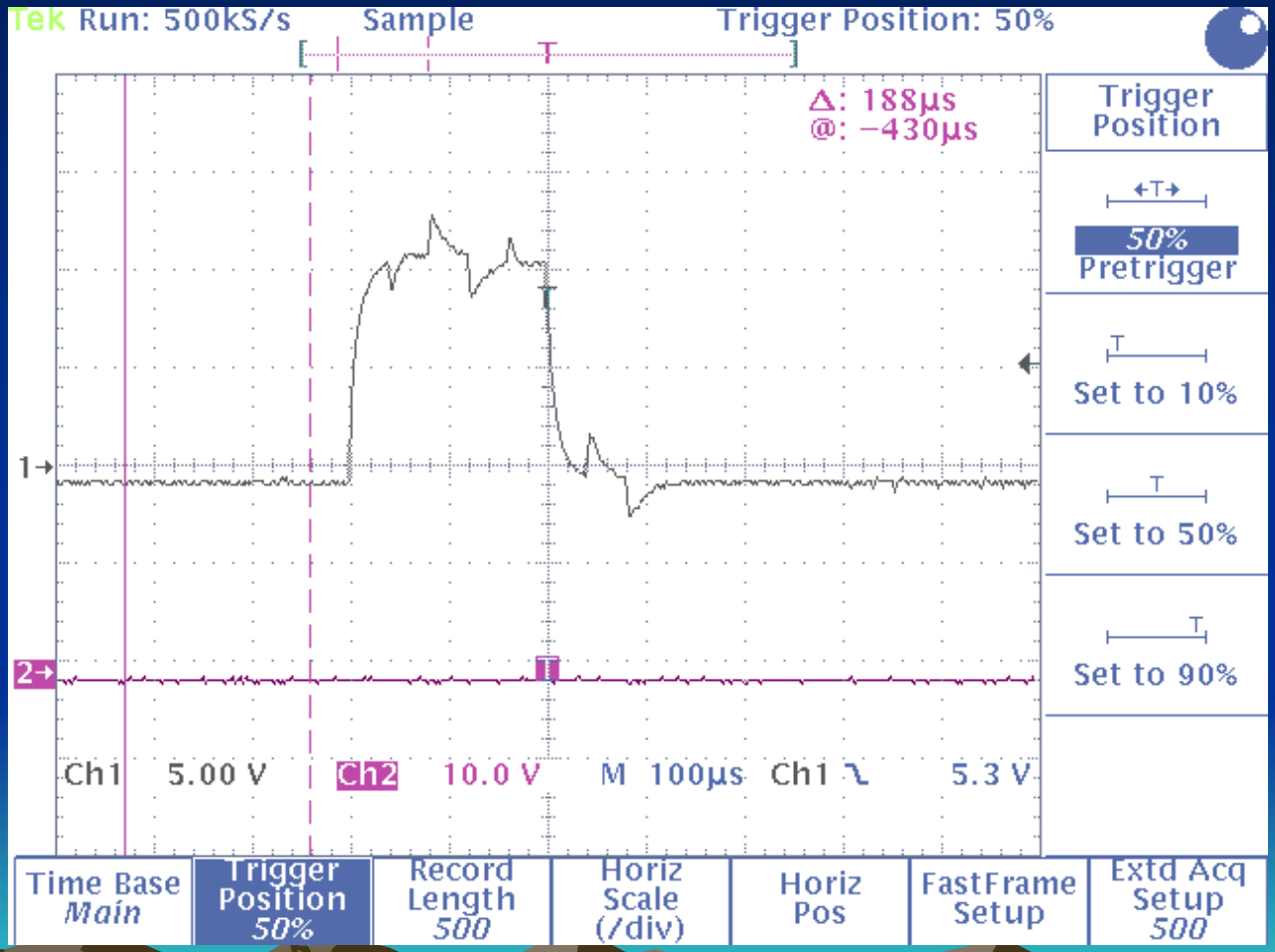
Pin 9 (D phase 2)



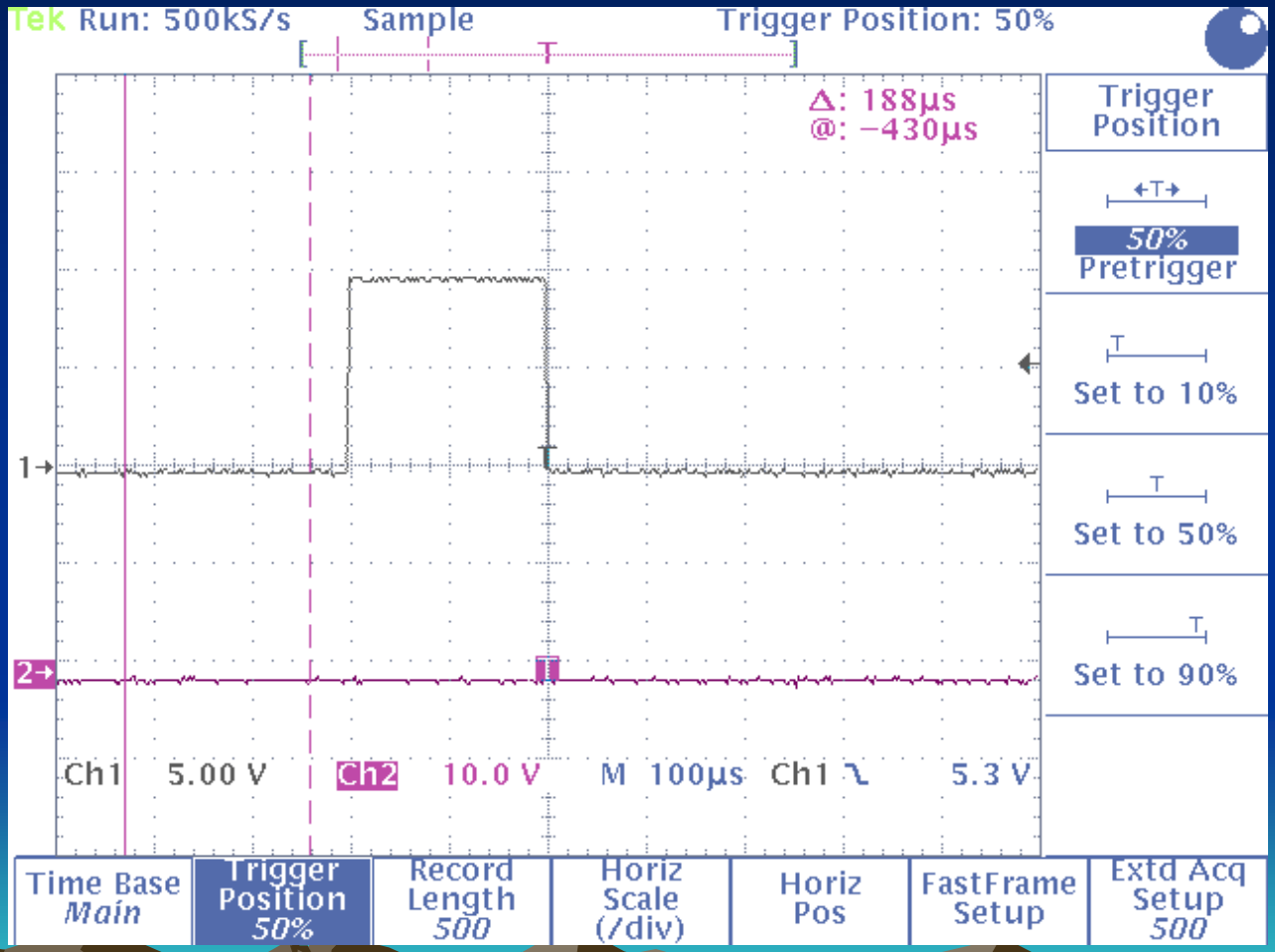
Pin 10 (D phase 3)



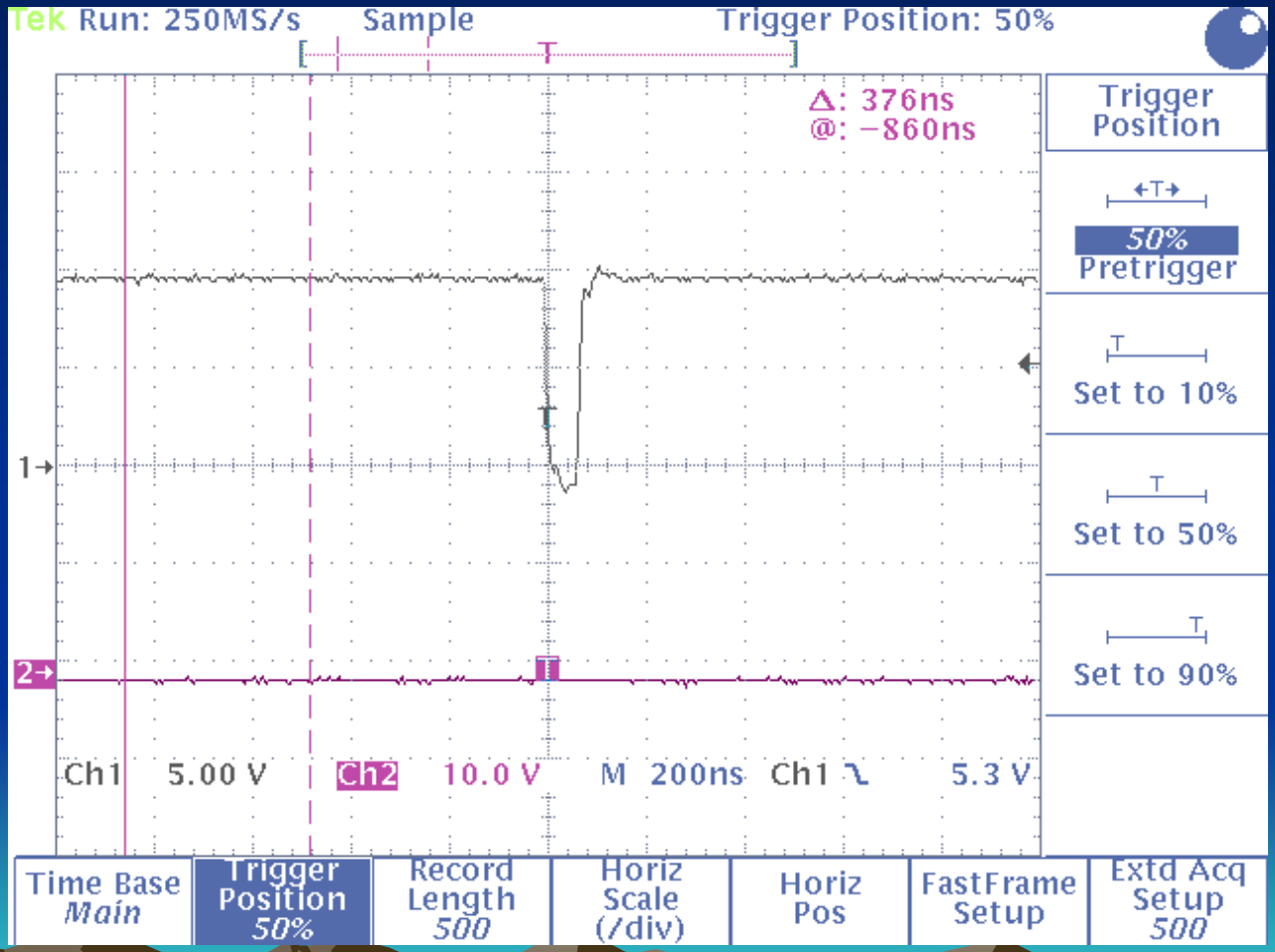
Pin 11 (D phase 4)



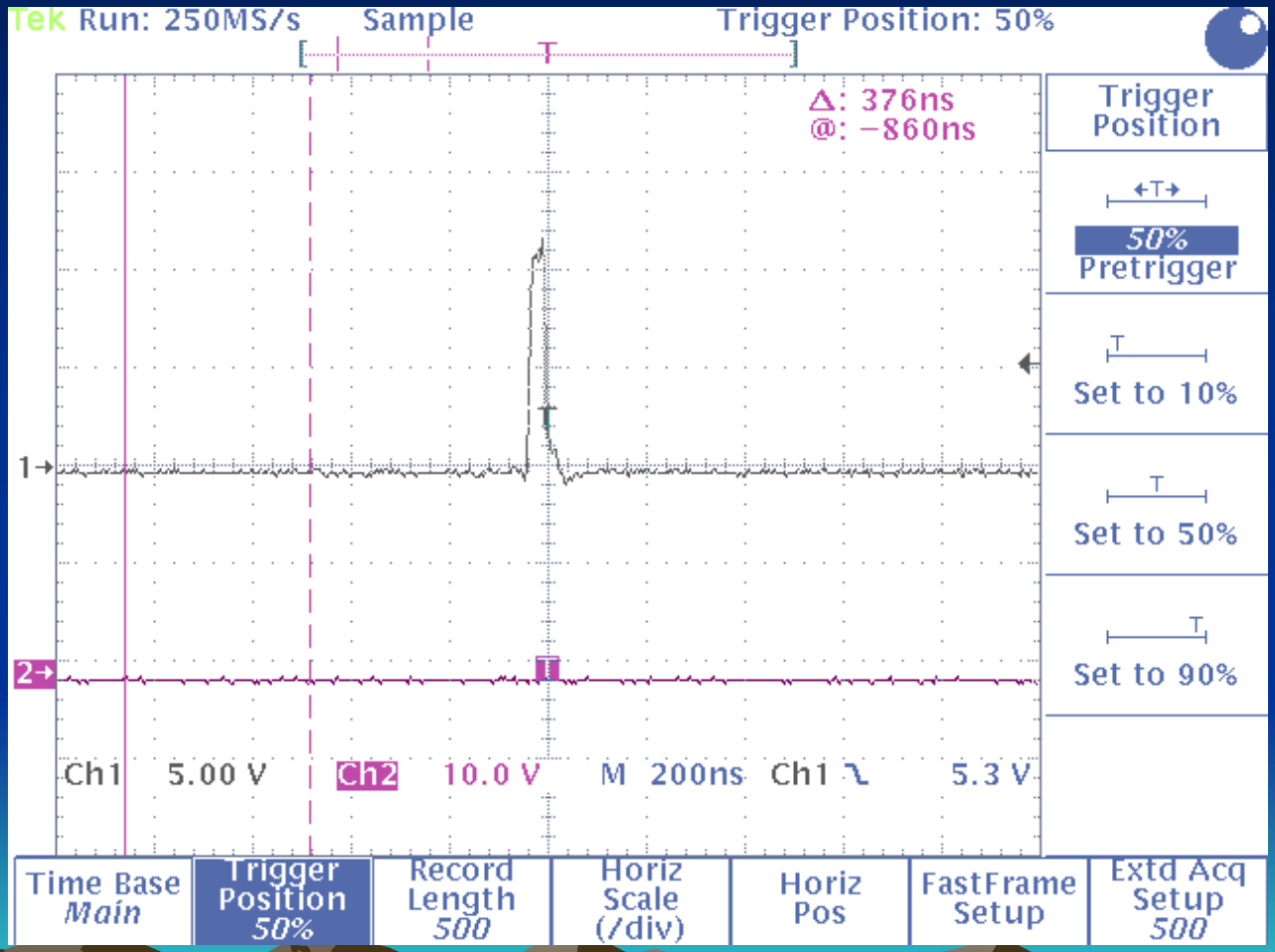
Pin 12 (Transfer Gate)



Pin 14 (Summing Well)



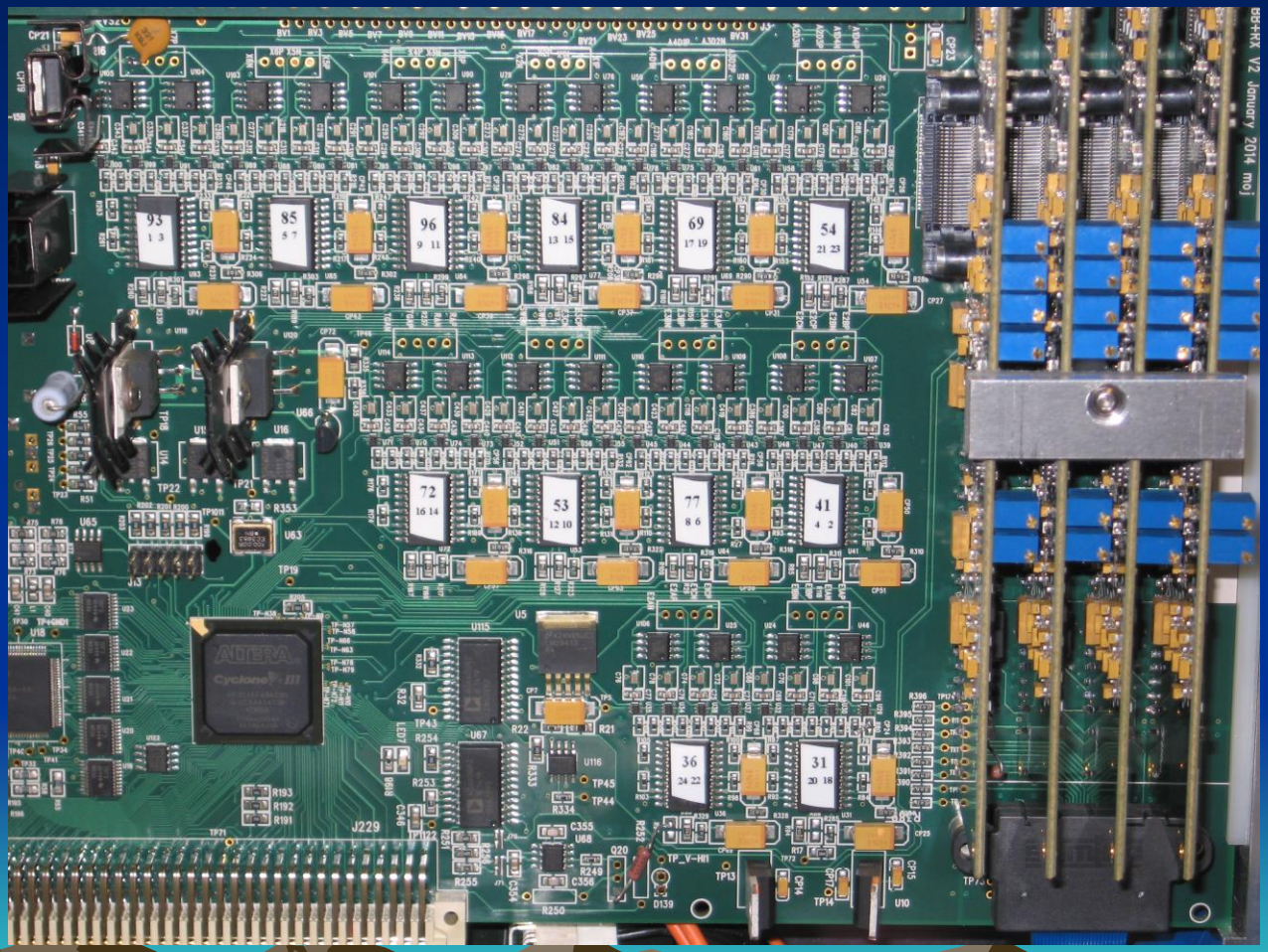
Pin 15 (Reset Gate)



Waveforms on the CBB

- The same waveforms can be observed on the Clock Bias Board
- Each of the Clock Driver Integrated Circuits (cdic) is has a white label
- The large number is the reference designator for that cdic
- The two small number correspond to the driver number (two for each integrated circuit) and are also the pin numbers in the blue cables

Clock Bias Board Clock Drivers



Clock Driver Circuits 1

- Below each cdic are two 43 Ohm resistors, one for each of the 24 clocks.
- The 43 Ohm resistors act as back terminators for the 50 Ohm cables to the CCD.
- The side of the resistor farther away from the cdic is connected to the CCD through the blue cables and the Wall Board

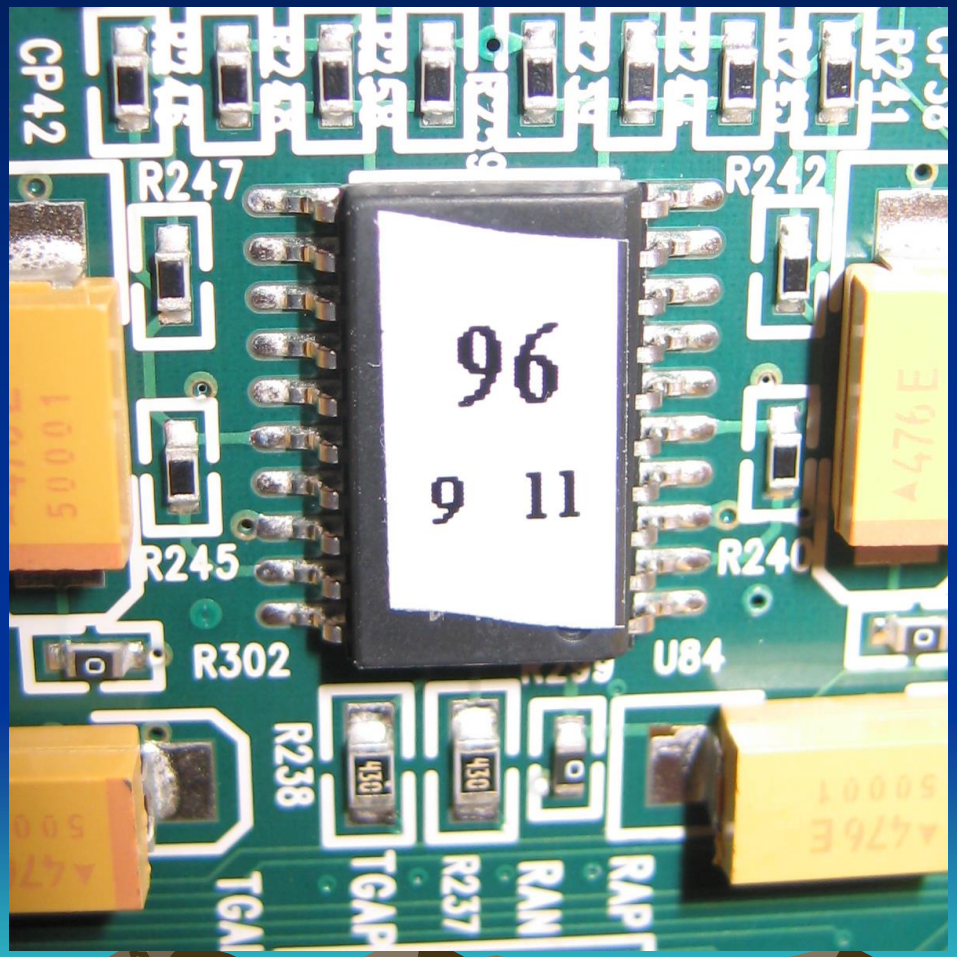
Clock Driver Circuits 2

- Probing the side of the resistor away from the cdic will give nearly the same waveform as shown above.
- Reflections from the CCD, which occur about 40 nsec after the drive signal, will be seen.
- The other side of the resistor is on the output of the cdic and will have clean square edges

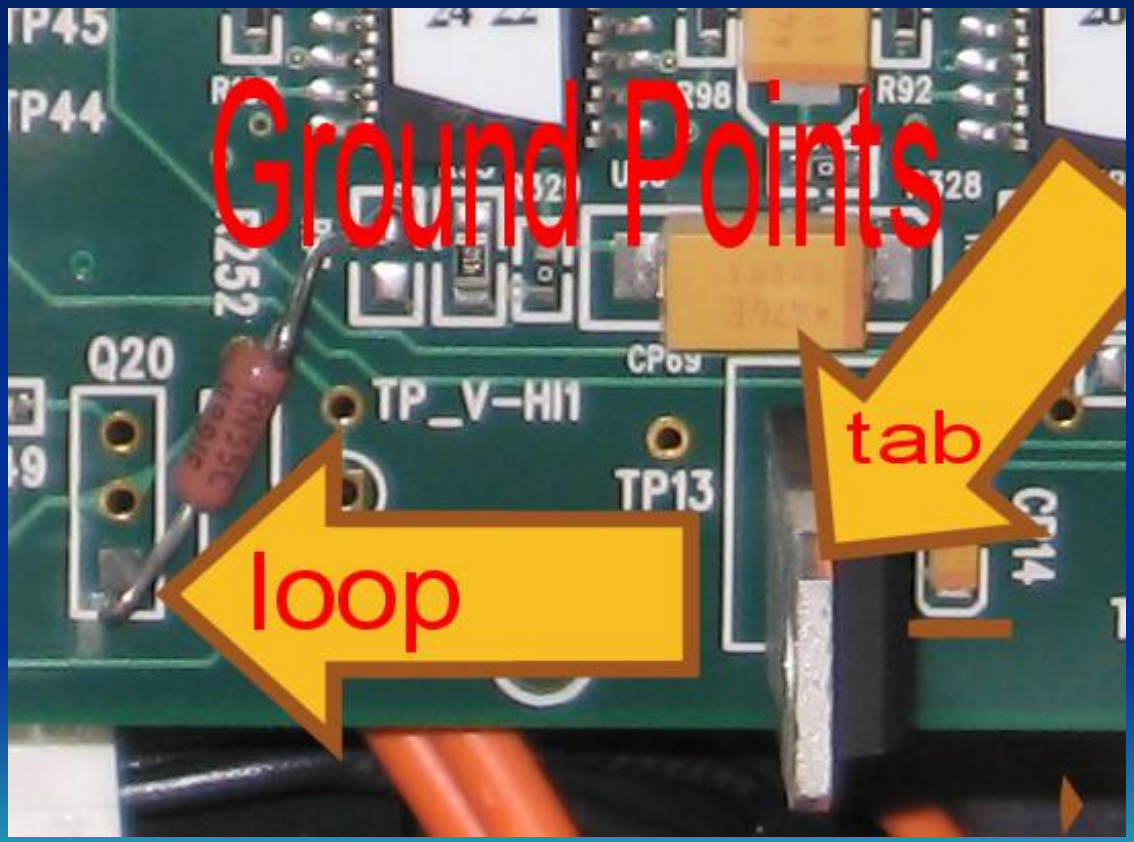
Detail of CDIC U96, clocks 9 and 11

- The photo below is a close-up of cdic U96
- The 43 Ohm resistors, R238 and R237 can be seen
- R238 corresponds to the pin 9 clock signal as indicated by the small number, bottom left, on the cdic label
- R237 corresponds to the pin 11 clock signal, as indicated by the small number, bottom right, on the cdic label

U96 detail



Possible ‘scope probe ground points for CBB



Caution

- Do not attempt to probe other parts of the CBB, especially the very dense area directly above each cdic.

DATE/By/n-of

CCD 290-99 on MK IV CBB

use:

ADR	TIME	CD	CC	CB	CA				
						stop /recycle	d31	HI/LO	a10
							d30	DAT/ADD	a9
							d29	WR/RD	a8
							d28	~W Strobe	a7
						ADC go	d27		a6
							d26		a5
							d25		a4
							d24		a3
						PA hold	d23	OSUbus d7	b28
						PA signal int.	d22	OSUbus d6	b27
						PA base int.	d21	OSUbus d5	b26
						PA reset	d20	OSUbus d4	b25
						Dmy Signal	d19	OSUbus d3	b24
							d18	OSUbus d2	b23
						LED	d17	OSUbus d1	b22
						Prep	d16	OSUbus d0	b21
						p4 D	d15	pin 11 v11/v12	c28
						p3 D	d14	pin 10 v111/v12	c27
						p2 D	d13	pin 9 v11/v12	c26
						p1 D	d12	pin 8 v11/v12	c25
						p4 A	d11	pin 4 v9/v10	c24
						p3 A	d10	pin 3 v9/v10	c23
						p2 A	d9	pin 2 v9/v10	c22
						p1 A	d8	pin 1 v9/v10	c21
							d7		a28
						TG A	d6	pin 12 v7/v8	a27
						RG E	d5	pin 15 v5/v6	a26
						SW E	d4	pin 14 v3/v4	a25
							d3		a24
						S3-E	d2	pin 7 v1/v2	a23
						S2-E	d1	pin 6 v1/v2	a22
						S1-E	d0	pin 5 v1/v2	a21

a 1010
b 1011
c 1100
d 1101
e 1110
f 1111

rev A 2013/3/1
description

DATE/By/n-of

CCD 47-20 on MK IV CBB

use:

ADR	TIME	CD	CC	CB	CA				
						stop /recycle	d31	HI/LO	a10
							d30	DAT/ADD	a9
							d29	WR/RD	a8
							d28	~W Strobe	a7
						ADC go	d27		a6
							d26		a5
							d25		a4
							d24		a3
						PA hold	d23	OSUbus d7	b28
						PA signal int.	d22	OSUbus d6	b27
						PA base int.	d21	OSUbus d5	b26
						PA reset	d20	OSUbus d4	b25
						Dmy Signal	d19	OSUbus d3	b24
							d18	OSUbus d2	b23
						LED	d17	OSUbus d1	b22
							d16	OSUbus d0	b21
							d15	pin 11 v11/v12	c28
						I3	d14	pin 10 v111/v12	c27
						I2	d13	pin 9 v11/v12	c26
						I1	d12	pin 8 v11/v12	c25
							d11	pin 4 v9/v10	c24
						S3	d10	pin 3 v9/v10	c23
						S2	d9	pin 2 v9/v10	c22
						S1	d8	pin 1 v9/v10	c21
						Micro/Macro SEQ	d7		a28
						TG A	d6	pin 12 v7/v8	a27
						RG E	d5	pin 15 v5/v6	a26
						SW E	d4	pin 14 v3/v4	a25
						do a micro pix	d3		a24
						R3R/R3/L	d2	pin 7 v1/v2	a23
						R2R/R1L	d1	pin 6 v1/v2	a22
						R1R/R2L	d0	pin 5 v1/v2	a21

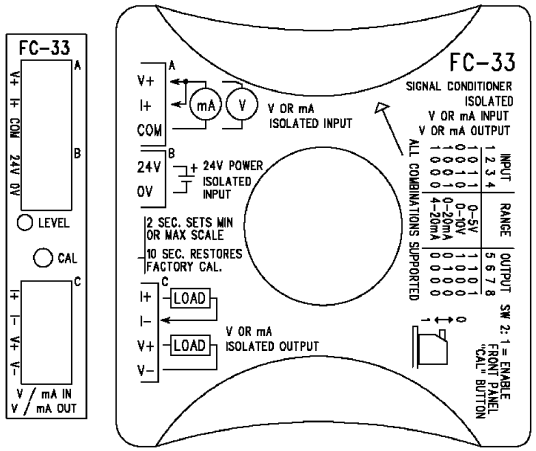
a 1010
b 1011
c 1100
d 1101
e 1110
f 1111

rev A 2013/3/1
description

FACTS engineering

FC-33

DC Selectable Input, Isolated Signal Conditioner



Description

The FC-33 is a DIN rail mount, selectable input / output signal conditioner with 1500VDC isolation between input and output and 1500VDC isolation from 24 volt power and input / output. The field configurable input/output types allow a wide ranging capability for 0 - 5V, 0 - 10V, 0 - 20mA, 4 - 20mA.

The FC-33 has user selectable factory-calibration, but also has OFFSET (zero) and SPAN (full scale) adjustments of the input signal. The OFFSET (zero) has an adjustment range of 0 to 25% of full scale input, the SPAN (full scale) has an adjustment of 80 to 102%

Application

The FC-33 field configurable isolated input/output signal conditioner is useful in eliminating ground loops and interfacing sensors to our PLC analog input modules. The FC-33 has 3 way isolation, this feature solves many types of configuration problems. For example, the signal conditioner can be configured for sinking input and sourcing output. It also allows signal translation from current input to voltage output or voltage input to current output.

This feature would be useful when you have limited type and number of channels in your system design, i.e. 8 channels of 4-20mA, 7 which are used and one transmitter that is 0 - 10V.

LEVEL LED

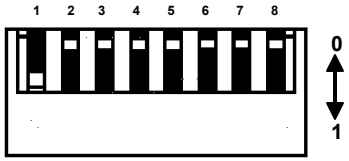
This LED is a powerful tool when setting up the signal conditioner. During normal operation the LED will blink at a proportional rate to the selected input signal level. When performing field calibration the LED is used for indication of the internal calibration process.

CAL - Pushbutton

This pushbutton along with various switch settings, allows you to calibrate the signal conditioner for your application or restore factory default calibration.

Input Selection

The signal conditioner can be configured for either DC milliamps or DC volts. Input and Output signal types are 0 - 5V, 0 - 10V, 0 - 20mA, 4 - 20mA.



example:
4 - 20mA input
4 - 20mA output

Input Ranges	Output Ranges	Switch Position							
		1	2	3	4	5	6	7	8
0 - 5V		1	0	1	1				
0 - 10V		0	0	1	0				
0 - 20mA		1	0	0	1				
*4 -20mA		1	0	0	0				
	0 - 5V					1	1	0	1
	0 - 10V					1	0	0	0
	0 - 20mA					0	1	0	0
	4 - 20mA					0	0	0	0
Factory Default Settings									
4 - 20mA	4 - 20mA	1	0	0	0	0	0	0	0

* Must connect jumper from V+ to I+ for current input.

Specifications	
Input Ranges	0-5V, 0-10V, 0-20mA, 4-20mA
Input impedance	250Ω ±0.1% current input 200KΩ / 400KΩ Voltage Input
Output Ranges	0-5V, 0-10V, 0-20mA, 4-20mA
Load Impedance	2KΩ minimum, voltage output 0Ω minimum, current output
Maximum Load / Current	550Ω @ 24V sink/source
Sample Duration Time	10mS
Filter Characteristic	-3dB @ 3Hz, -6dB/octave
Linearity Error	0.05% FSO maximum
Stability	0.05% FSO maximum

Note: All data 0° - 60° C except where specified.
[1] Internal Analog convertor resolution is 12 - bit.

CAUTION: PRODUCT MAY BE DAMAGED IF CURRENT OUTPUT (I+/I-) AND VOLTAGE OUTPUT(V+/V-) ARE BOTH CONNECTED TO LOADS. DO NOT TIE THE I+ TERMINAL TO THE V- TERMINAL.

Adjustments

The FC-33 has built-in self-calibration, but also has OFFSET (zero) and SPAN (full scale) adjustments of the input signal. If your application requires, different span or offset (i.e. 3.6mA offset and 19.6mA span) you can adjust accordingly.

Application adjustments

Calibrating the input signal level -

1. Select the signal range (i.e. 4 - 20mA).
2. Connect 24 volt power to the signal conditioner.
3. Connect the minimum input signal level.
4. Turn Switch **2 ON**, press and hold the CAL pushbutton until the LEVEL LED comes ON steady (approx. 3 seconds), then release immediately. If the pushbutton is NOT released while the Level LED is ON steady, the signal conditioner will return to factory calibration.
5. Repeat above sequence for maximum input signal.
6. Turn Switch **2 OFF.**

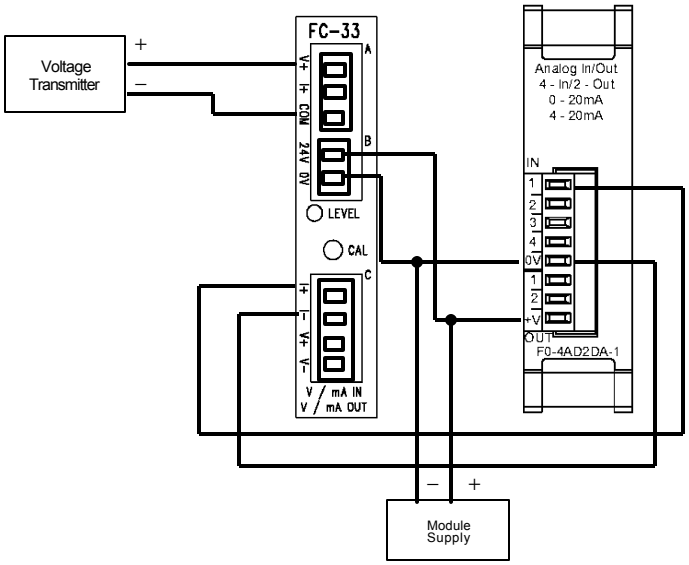
To return to factory calibration-

1. Turn switch **2 ON**, press and hold the CAL pushbutton until the LEVEL LED comes ON steady and then starts flashing (approx. 10 seconds), then release the pushbutton. The unit has now been returned to factory calibration.
2. Turn Switch **2 OFF.**

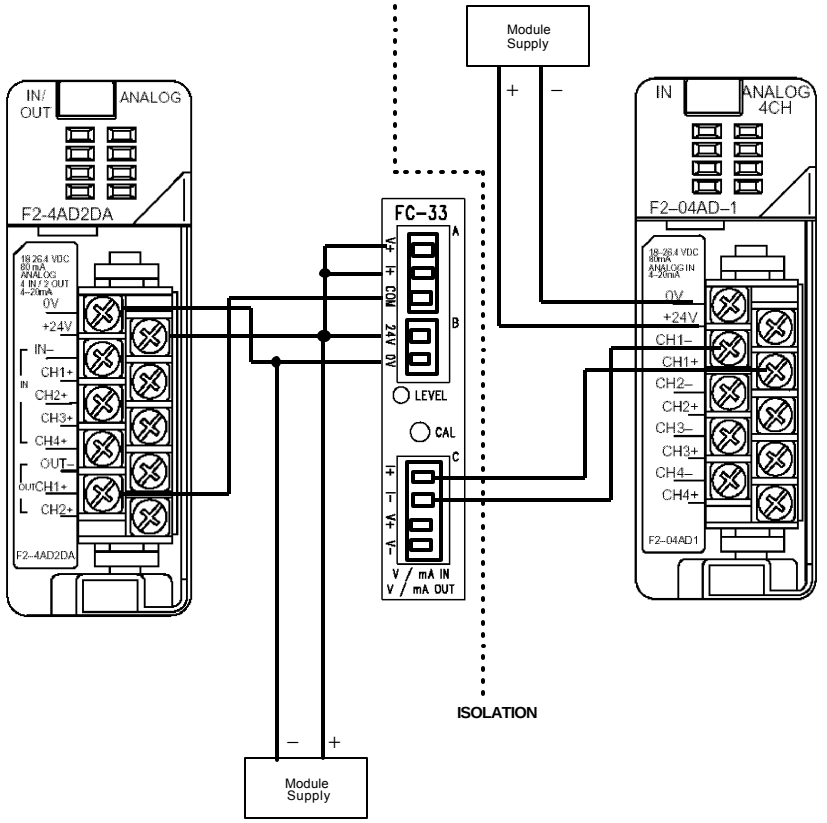
General Specifications	
Accuracy vs. Temperature	± 0.005% / °C (50ppm/°C)
Input Power	24VDC ±10% @ 50mA
Recommended Fuse	0.032A Littelfuse Series 217 current inputs
Isolation	1500VDC input - output 1500VDC power - input 1500VDC power - output * applied for 1 second
Maximum Inaccuracy of output (Includes offset,span,linearity)	0.05% FSO @ 25°C 0.25% FSO @ 0 - 60°C
Output Current	21mA maximum (for mA output)
Approx. field cal. range	0 - 25% (0 - 1.5V / 5V mode) 80% - 102% (4 - 5.1V / 5V mode)

Operating Temperature	0 to 60°C (32 to 140°F)
Storage Temperature	-20 to 70°C (-4 to 158°F)
Relative Humidity	5 to 90% (non-condensing)
Environmental air	No corrosive gases permitted
Vibration	MIL STD 810C 514.2
Shock	MIL STD 810C 516.2
Noise Immunity	NEMA ICS3-304

Typical Connection -



Voltage Input and Current Output (example)



4 - 20 mA Sinking Output to Isolated 4-20 mA Sinking Input (example)

THIS EQUIPMENT IS SUITABLE FOR USE IN CLASS I, DIVISION 2, GROUPS A, B, C AND D OR NON-HAZARDOUS LOCATIONS ONLY.
WARNING – EXPLOSION HAZARD - SUBSTITUTION OF COMPONENTS MAY IMPAIR SUITABILITY FOR CLASS I, DIVISION 2 / ZONE 2.
WARNING – EXPLOSION HAZARD - DO NOT DISCONNECT EQUIPMENT UNLESS POWER HAS BEEN SWITCHED OFF OR THE AREA IS KNOWN TO BE NON-HAZARDOUS.