Common Mode Rejection Ratio (CMRR)
and
Overscan level depending on Flat Field level

CCD signal processing for KMTN

The signal from a CCD is the result of transferring a packet of charge to the output node. The output node is well modeled as a small capacitor, of the order of 10fF. The charge packet from each pixel is taken to be proportional to the total flux of light that fell on a pixel during the exposure. The Voltage shift on the output node is then also proportional to the exposure and given by $V=Q/C$ where V is the decrease (decrease in the case of CCDs that transfer electrons, it is positive for devices that transfer holes) in Voltage on the output node, Q is the charge in the packet from a given pixel and C is the capacity of the output node. The Voltage on the output node is buffered by an on-chip amplifier with a Voltage gain of about 0.5 The output node must be reset prior to transferring the charge packet to erase the effect of reading previous pixels. This reset process leaves the exact Voltage on the output node uncertain by a Voltage that corresponds to ~50 electrons for the KMTN CCDs. This uncertainty is the result of the Johnson noise of the switch used to reset the output node capacity, there are no tricks to eliminate it. The solution is to measure the Voltage on the output node after resetting the output node and subtract it from the Voltage on the output node after the charge packet is transferred. To the degree that the Voltage noise from the on-chip amplifier is white, the optimal filter to measure that level is to integrate the signal for as long as you can. The usual overall solution is to use a dual slope integrator, that is: integrate the reset level for a time *t*, stop integrating and hold the level, transfer the charge to the output node, continue the integral for another time *t* after *inverting the signal*. In practice the analog integrator is fed from three analog switches. One is connected to signal from the output node amplified with a gain of +5, the second in connected to the signal from the output node amplified with a gain of -5, and the third connected to ground. The components of the integrator are selected for the time-constant of 750 nsec. Prior to transferring the signal to the output node the signal amplified by +5 is integrated for 733 nsec. During the time the charge packet is transferred to the output node and the amplifiers settle the input to the integrator is connected to ground. The integration is then continued for another 733 nsec but with the input of the integrator connected to the signal amplified by -5. The net result of this simple model is that for any constant input Voltage the integrator output will be zero and the output will be proportional to the size of the step in Voltage on the output node when the charge packet is transferred. A small offset, adjustable with RV 6 and RV3, is added to the output of the integrator before it is sent to the Analog to Digital Converter.

The matching of the gain of +5 and -5 is what makes the output of the dual slope integrator zero for any constant, no step, input Voltage. That matching is frequently characterized as a Common Mode Rejection Ratio (CMRR). The CMRR for the KMTN post amplifiers is adjustable with RV1 and RV4.

If the entire signal chain form output node to ADC were DC coupled, and stable, a very high CMRR would not be required. However the Voltage from output node of modern CCDs typical has a DC component of ~25 Volts. There are methods to subtract off such a large Voltage with sufficient stability to allow end-to-end DC coupling, but they are complex and troublesome. The KMTN system is AC coupled, with a 0.1 second time constant, about 40,000 pixels. After a long series of bias pixels the output of the AC coupling settles near zero Volts. However after a long series of "bright" pixels, as when reading a flat field, the output is an asymmetric square wave with a level above zero (positive) prior to transferring the signal and below zero (negative) after transferring the charge tot he output node. In practice the DC level during the baseline integration can be more that 1 Volt. If after the long series of bright pixels the dual-slope - integrator starts receiving bias pixels the DC level will decay back to zero with the AC coupling time constant, about 40,000 pixels. If the dual-slope-integrator is to produce the correct bias level during the time the DC Voltage is decaying back to zero the CMRR must be quite high. Obviously only with good CMRR will subsequent dark or overscan pixels be independent of the flat field level. The CMRR can be adjusted by injecting a slow (<1 Hz) triangle wave with a peak to peak amplitude of 300 mV and an offset of 150 mV just after C2 or C102 and adjusting the CMRR pots for minimum change in the output level as seen with the real-time program. Typically the CMRR can be trimmed so that only second order changes are present as seen by slight motion at *twice* the input frequency. To get the best results it is important to trim the CMRR over the correct range. I have made changes to the CBB firmware which reduces the time the signal is present on the output node, that is the time from the summing well clock, which is when the signal is transferred to the output node, to the CCD reset signal. It is now 933 nsec while the pixel time is 2.4 microsec thus the signal is present only 39% of the time. The responsivity of the output notes varies a few percent but is typically 7 microVolts per electron while the system gain is always less than 2 electrons per ADU. (Theoritical gain at the input to the PA is 12.84 microVolt/ADU. The responsivity values quoted by e2v should be reduced by about 6% due to the finite settling time at the input to the integrator.) In any event, there are only 65536 ADU available and 12.84 microVolts/ADC gives a maximum signal at the input of the PA of 841.5 mVolts which is present for at most 39% (28 of 72 cycles of the 30 MHz clock) of the time (less if you include the time required for vertical transfers) giving maximum DC level of 327.2 mVolts.

Comments on Cung-uk's observations of 3/19/2016 (12:43AM EDT)

Attached to Chung-uk's email are plots of overscan (OS) level as a function of flat-field (FF) level (actually presented with FF level on the vertical axis and OS level on the horizontal). In general the CMRR is quite good for most channels with a CMRR of ~10^3. There is, however, a strong trend for increasing OS level with increasing FF level. The CTIO shows ~7 channels (of 32) as outliers, some with large slope (some negative) and one that is wicked-bad with a CMRR of only ~20. (One possible explanation for the very poor performance of this channel is that the pot was accidentally turned full CCW. If that were the case turning the pot 6 turns CW would produce substantially better results.) SSO shows all 32 channels with CMRR of 1-2*10^3 and positive slope. I suspect the consistent modest positive slope in the SSO channels (and in most of the CTIO channels) is simply the result of optimizing the CMRR over the wrong range. I had

not previously done a careful calculation of the best range over which to adjust the CMRR. Using the procedure outlined above, and described more fully in the video, I achieve CMRRs of about 6000 while the limit, when using a much more time-consuming process, seems to be about 10,000. The limit is set by second order effects for which there is no adjustment.

My feeling is that the residuals are probably not important for normal observations since the residual is a function of the previous pixels averaged with a 40,000 pixel time constant. I've never done the test but I bet that this average, even in a crowded field, is not more than 10% of full scale.

What effect does this have on light curves? Again, my feeling is that it has none. I am assuming that the photometry is being done in such a way that stellar brightness is being measured with respect to local sky and any shift in bias is subtracted out.

If required in the data reduction, overscan should be used, not underscan. The underscan is there in part to get the pixel reading process started smoothly again after the inevitable transient caused by the vertical transfer.

Am I correct in assuming that the vertical parts of the plots on pages 9, 10, 11, and 12 are from saturated flat fields?

Am I correct in assuming that the plots on pages 3, 9, 10, 11, 12, 17, 18, 19, 20, 25, 26, 27, and 28 are underscan vs overscan?